

MODEL NAME : *Viking 18*  
PCB NO : *LA-9332P*  
BOM P/N : *4619KU31L01*

# Compal Confidential

## Viking 18

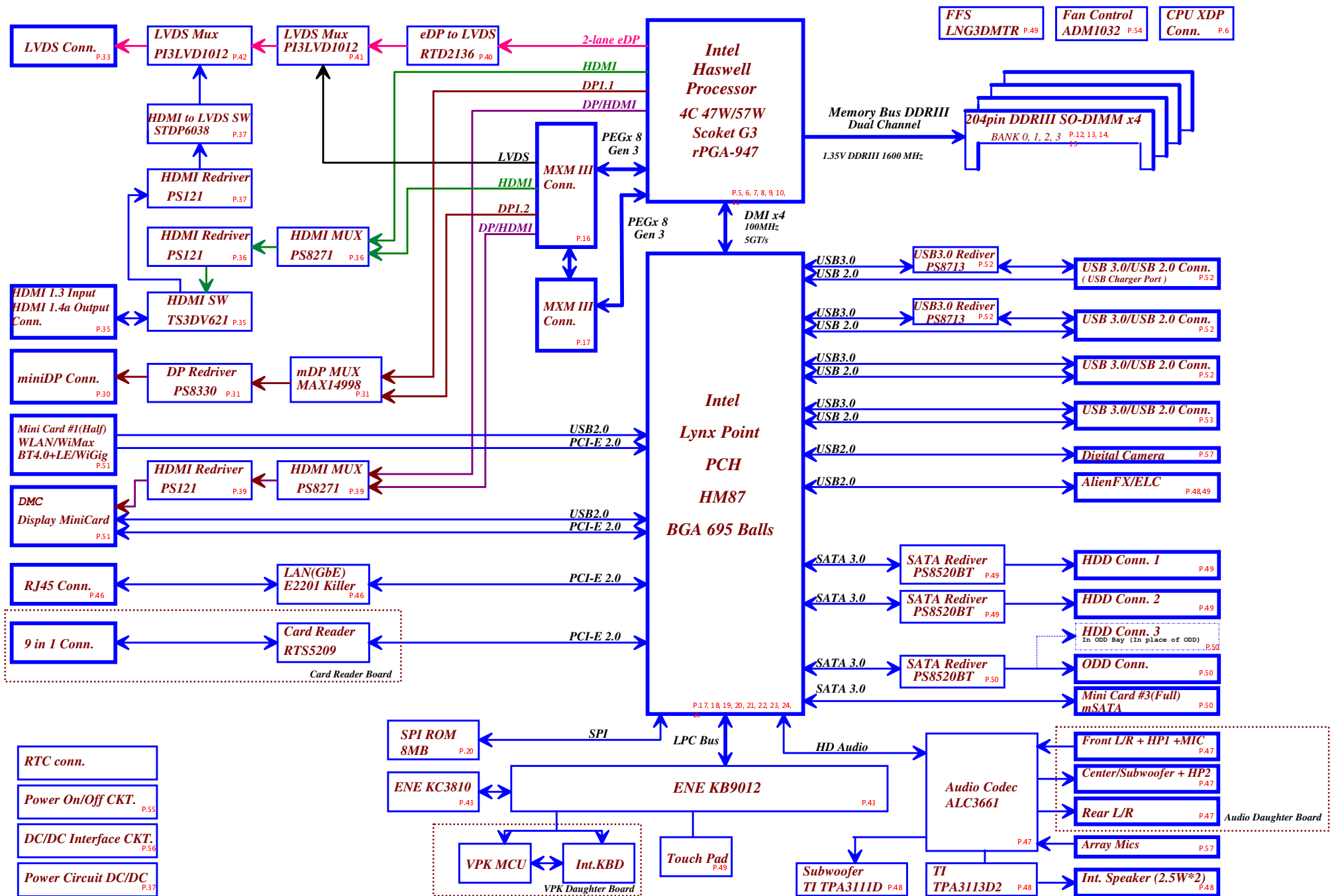
### Schematic Document

Rev: X02

2012-11-19

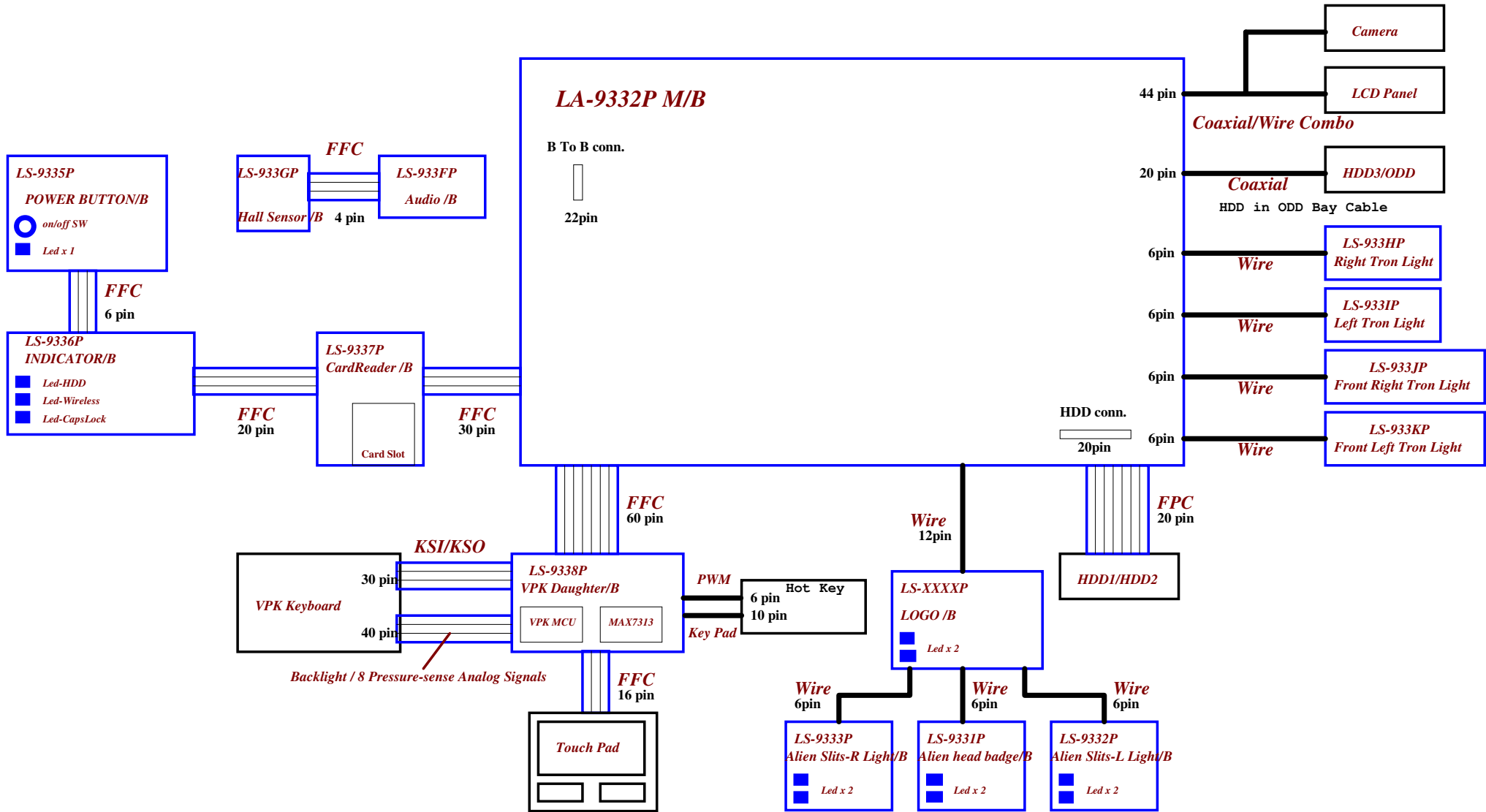
@ : Nopop Component

|  |                    |                 |            |  |               |
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| Issued Date  | 2012/05/14         | Deciphered Date | 2013/05/13 | Title                                  | Cover Sheet   |
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|  |                    |                 |            | Wperdf\INCIS\SPEC\BAS40-04_SOT23-3.pdf |               |
|  |                    |                 |            | Date: Friday, December 14, 2012        | Sheet 1 of 56 |



|  |            |                    |            |                 |     |
|--|------------|--------------------|------------|-----------------|-----|
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| Issued Date  | 2012/02/28 | Deciphered Date    | 2013/02/27 | Block Diagram   |     |
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|  |            |                    |            | LA-9332P        | 0.1 |
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Project Code : VAS10  
File Name : LA-9332P



Board ID Table for AD channel

|          |             |             |             |             |           |
|----------|-------------|-------------|-------------|-------------|-----------|
| Vcc      | 3.3V +/- 5% |             |             |             |           |
| Ra       | 100K +/- 5% |             |             |             |           |
| Board ID | Rb          | VAD_BID min | VAD_BID typ | VAD_BID max | EC AD3    |
| 0        | 0           | 0 V         | 0 V         | 0.155 V     | 0x00-0x0C |
| 1        | 8.2K +/- 5% | 0.168 V     | 0.250 V     | 0.362 V     | 0x0D-0x1C |
| 2        | 18K +/- 5%  | 0.375 V     | 0.503 V     | 0.621 V     | 0x1D-0x30 |
| 3        | 33K +/- 5%  | 0.634 V     | 0.819 V     | 0.945 V     | 0x31-0x49 |
| 4        | 56K +/- 5%  | 0.958 V     | 1.185 V     | 1.359 V     | 0x4A-0x69 |
| 5        | 100K +/- 5% | 1.372 V     | 1.650 V     | 1.838 V     | 0x6A-0x8E |
| 6        | 200K +/- 5% | 1.851 V     | 2.200 V     | 2.420 V     | 0x8F-0xBB |
| 7        | NC          | 2.433 V     | 3.300 V     | 3.300 V     | 0xBC-0xFF |

BOARD ID Table

| Board ID | PCB Revision |
|----------|--------------|
| 0        | 0.1 (SSI)    |
| 1        | 0.2 (PT)     |
| 2        | 0.3 (ST)     |
| 3        | 0.4 (QT)     |
| 4        | 1.0 (MP)     |
| 5        |              |
| 6        |              |
| 7        |              |

| USB 3.0 PORT | Connction          |
|--------------|--------------------|
| 1            | JUSB1 (Right side) |
| 2            | JUSB2 (Right side) |
| 3            | NA                 |
| 4            | NA                 |
| 5            | JUSB3 (Left side)  |
| 6            | JUSB4 (Left side)  |

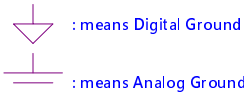
POWER STATES

| State                        | Signal | SLP S3# | SLP S4# | SLP S5# | S4 STATE# | SLP M# | ALWAYS PLANE | SUS PLANE | RUN PLANE | CLOCKS |
|------------------------------|--------|---------|---------|---------|-----------|--------|--------------|-----------|-----------|--------|
| S0 (Full ON) / M0            |        | HIGH    | HIGH    | HIGH    | HIGH      | HIGH   | ON           | ON        | ON        | ON     |
| S3 (Suspend to RAM) / M-OFF  |        | LOW     | HIGH    |         | HIGH      | LOW    | ON           | ON        | OFF       | OFF    |
| S4 (Suspend to DISK) / M-OFF |        | LOW     | LOW     | HIGH    | LOW       | LOW    | ON           | OFF       | OFF       | OFF    |
| S5 (SOFT OFF) / M-OFF        |        | LOW     | LOW     | LOW     | LOW       | LOW    | ON           | OFF       | OFF       | OFF    |

PM TABLE

| State                | power plane | +5VALW<br>+3VALW<br>+3VLP<br>+3V_PCH | +1.35V<br>+1.05V | +5VS<br>+3VS<br>+1.5VS<br>+1.05VS<br>+0.675VS<br>+3VMXM<br>+5VMXM<br>+VCC_CORE<br>+1.35V_CPU_VDDQ |
|----------------------|-------------|--------------------------------------|------------------|---|
| S0                   |             | ON                                   | ON               | ON  |
| S3                   |             | ON                                   | ON               | OFF   |
| S5 S4/AC             |             | ON                                   | OFF              | OFF   |
| S5 S4/AC don't exist |             | OFF                                  | OFF              | OFF   |

Symbol Note :



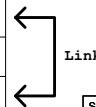
| CLK | DIFFERENTIAL | DESTINATION      | FLEX CLOCKS | DESTINATION |
|-----|--------------|------------------|-------------|-------------|
|     | CLKOUT_PCIE0 | MINI CARD-1 WLAN | CLKOUTFLEX0 | None        |
|     | CLKOUT_PCIE1 | MINI CARD-2 DMC  | CLKOUTFLEX1 | None        |
|     | CLKOUT_PCIE2 | 10/100/1G LAN    | CLKOUTFLEX2 | None        |
|     | CLKOUT_PCIE3 | CARD READER      | CLKOUTFLEX3 | None        |
|     | CLKOUT_PCIE4 | None             |             |             |
|     | CLKOUT_PCIE5 | None             |             |             |
|     | CLKOUT_PCIE6 | None             |             |             |
|     | CLKOUT_PCIE7 | None             |             |             |
|     | CLKOUT_PEG_A | MXM              |             |             |

| SATAIII          | DESTINATION      |
|------------------|------------------|
| SATA0            | HDD1             |
| SATA1            | HDD2             |
| SATA2            | ODD              |
| SATA3            | mSATA            |
| SATA4/PCIE LANE1 | MINI CARD-1 WLAN |
| SATA5/PCIE LANE2 | MINI CARD-2 DMC  |

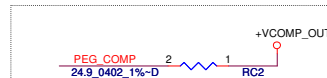
| PCI EXPRESS          | DESTINATION   |
|----------------------|---------------|
| Lane 1/USB3.0 Port 3 | None          |
| Lane 2/USB3.0 Port 4 | None          |
| Lane 3               | 10/100/1G LAN |
| Lane 4               | CARD READER   |
| Lane 5               | None          |
| Lane 6               | None          |
| Lane 7               | None          |
| Lane 8               | None          |

SMBUS Control Table

|                             | SOURCE | WLAN | DMC | BATT | DIMM | 6038 | 4028 | Thermal Sensor | FFS | 2136 | VPK MCU | MXM | XDP | Charger | TP | mSATA |
|-----------------------------|--------|------|-----|------|------|------|------|----------------|-----|------|---------|-----|-----|---------|----|-------|
| EC_SMB_CK1<br>EC_SMB_DA1    | KB9012 |      |     | V    |      |      |      |                |     |      |         | V   |     | V       |    |       |
| EC_SMB_CK2<br>EC_SMB_DA2    | KB9012 |      |     |      |      | V    | V    | V              |     | V    | V       |     |     |         |    |       |
| PCH_SMLCLK<br>PCH_SML0DATA  | PCH    |      |     |      |      |      |      |                |     |      |         |     |     |         |    |       |
| PCH_SML1CLK<br>PCH_SML1DATA | PCH    |      |     |      |      |      |      |                |     |      |         |     |     |         |    |       |
| MEM_SMBCLK<br>MEM_SMBDATA   | PCH    |      | V   |      | V    |      |      |                | V   |      |         |     | V   | V       | V  | V     |

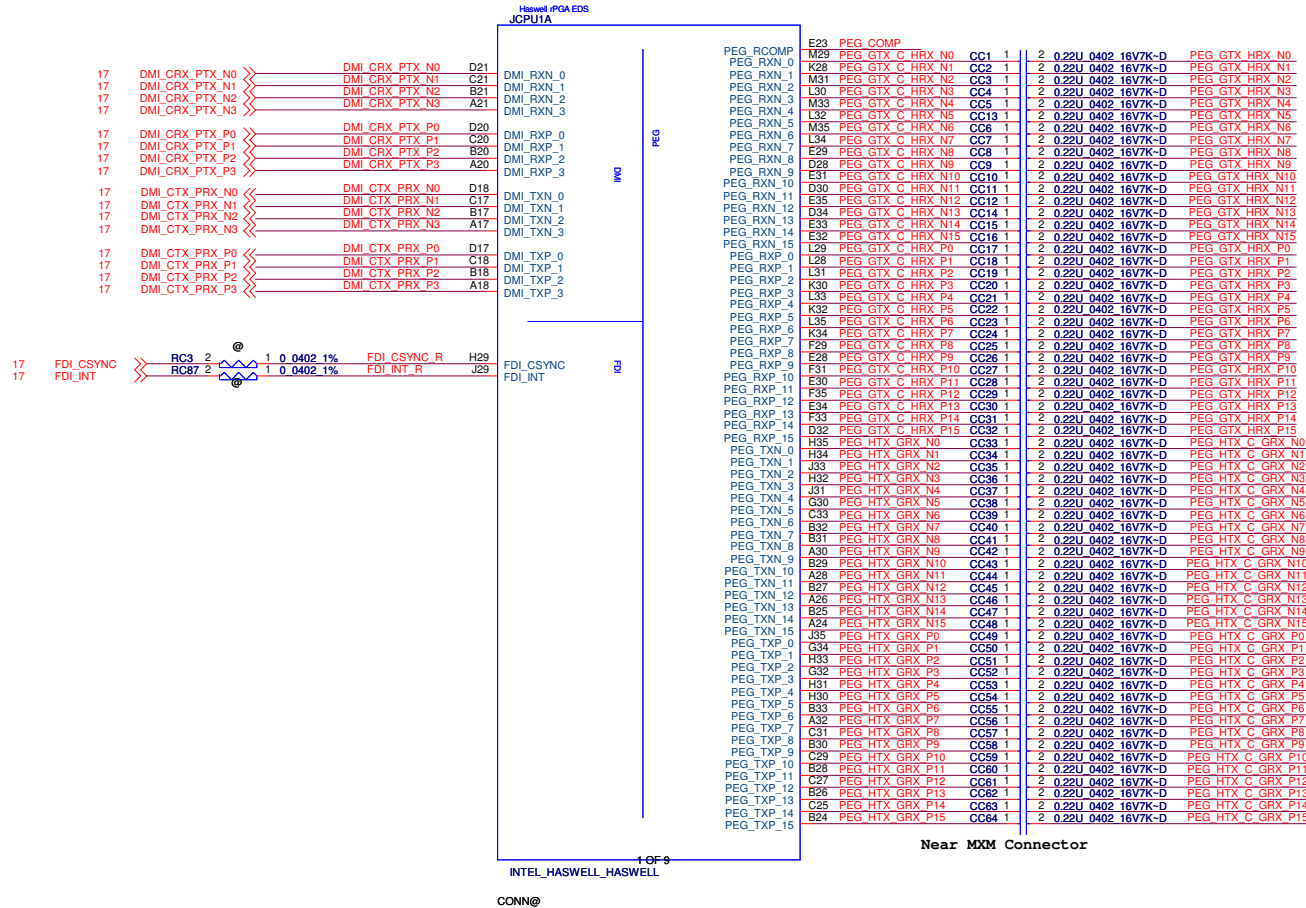


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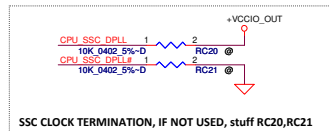
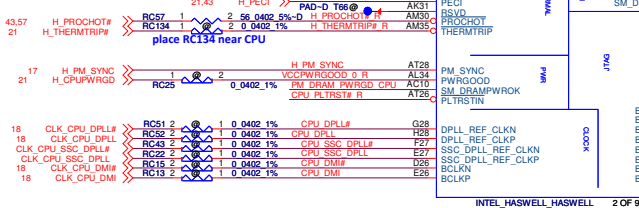
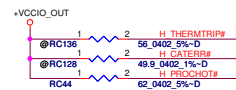
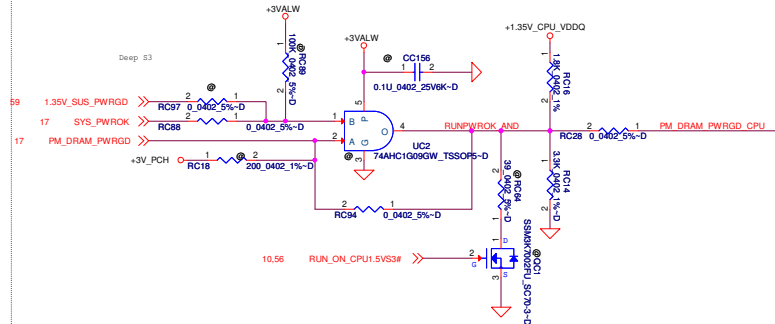
CAD Note:  
Trace width=12 mils ,Spacing=15mil  
Max length= 400 mils.

PEG\_GTX\_HRX\_P[0..15] 29.30  
PEG\_GTX\_HRX\_N[0..15] 29.30  
PEG\_HTX\_C\_GRX\_P[0..15] 29.30  
PEG\_HTX\_C\_GRX\_N[0..15] 29.30

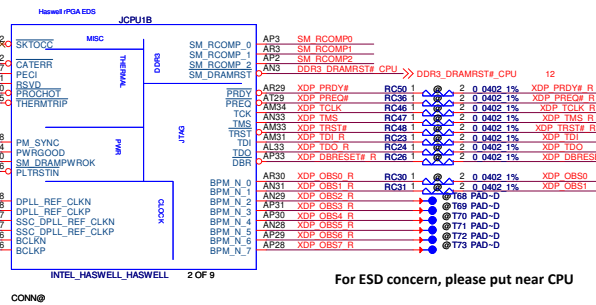
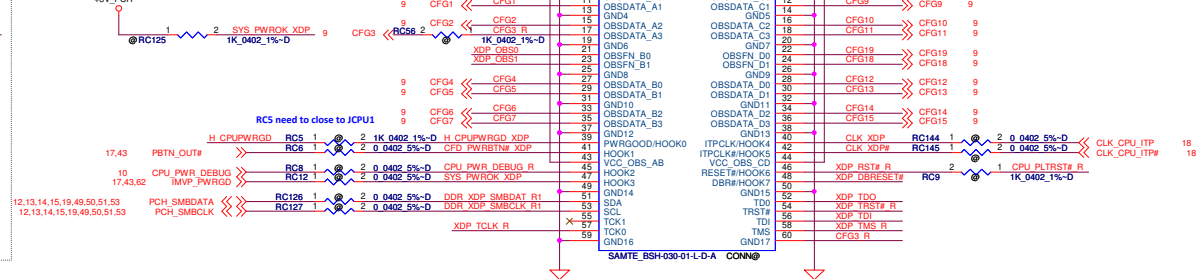
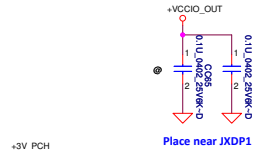
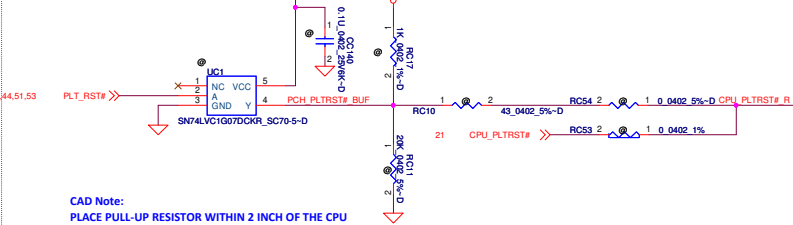


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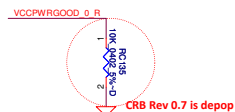
## SM\_DRAMPWROK with DDR Power Gating Topology



### Buffered reset to CPU



For ESD concern, please put near CPU



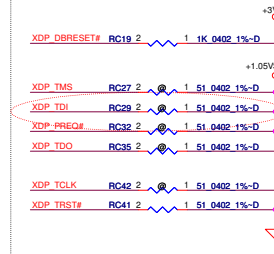
**CAD Note:**  
Avoid stub in the PWRGD path  
while placing resistors RC25 & RC130

## DDR3 COMPENSATION SIGNALS

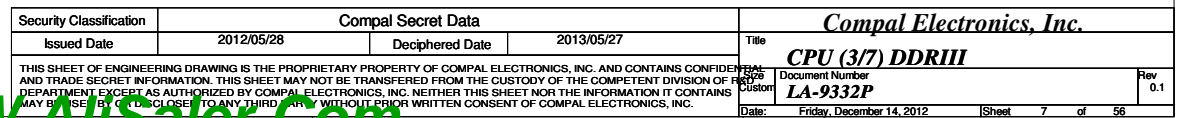


**CAD Note:**  
Trace width=12~15 mil, Spcing=20 mils  
Max trace length= 500 mil

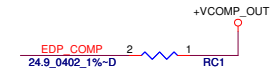
## PU/PD for JTAG signals



|   |                           |                 |  |                          |
|---|---------------------------|-----------------|--|--------------------------|
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| Date:   | Friday, December 14, 2012 | Sheet           | 6  | of 56                    |



## COMPENSATION PU FOR eDP

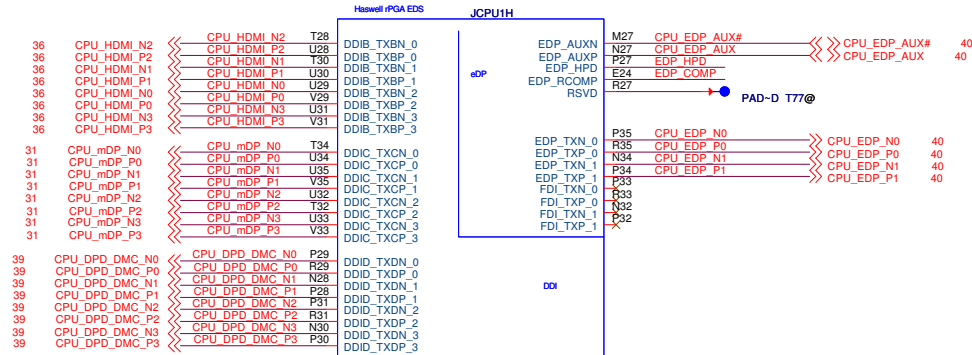


CAD Note: Trace width=20 mils ,Spacing=25mil,  
Max length=100 mils.

HDMI

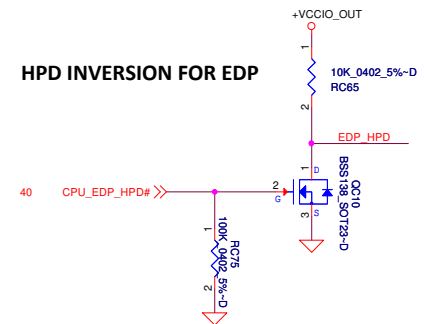
mDP

DMC



CONN@

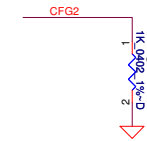
## HPD INVERSION FOR EDP



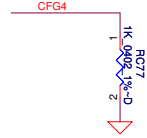
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|   |                    |                 |            | Rev                      | 0.1                       |



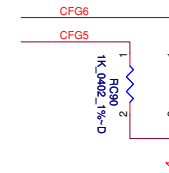
# CFG STRAPS for CPU



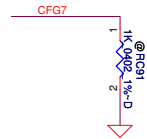
| PEG Static Lane Reversal - CFG2 is for the 16x |   |
|--|---|
| CFG2   | 1:(Default) Normal Operation; Lane # definition matches socket pin map definition<br>0: Lane Reversed |



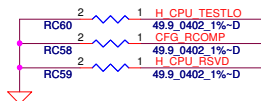
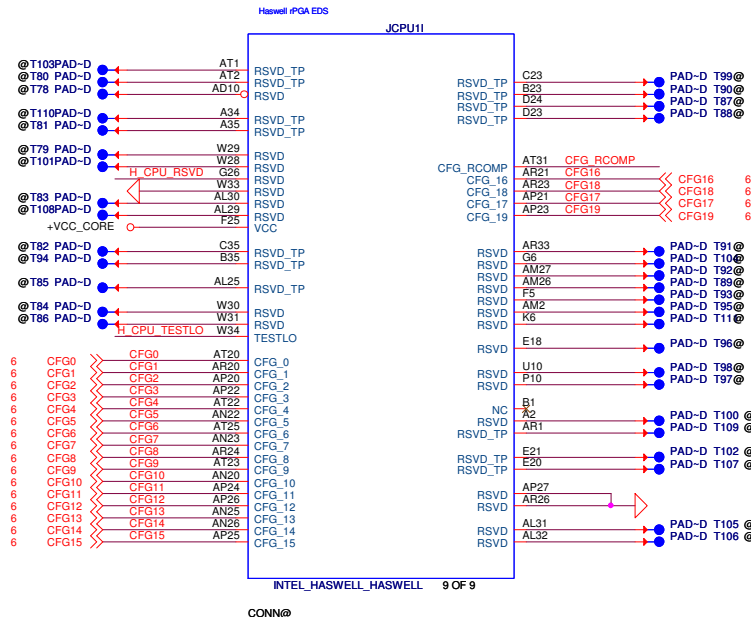
| Display Port Presence Strap |  |
|-----------------------------|--|
| CFG4                        | 1 : Disabled; No Physical Display Port attached to Embedded Display Port<br>0 : Enabled; An external Display Port device is connected to the Embedded Display Port |

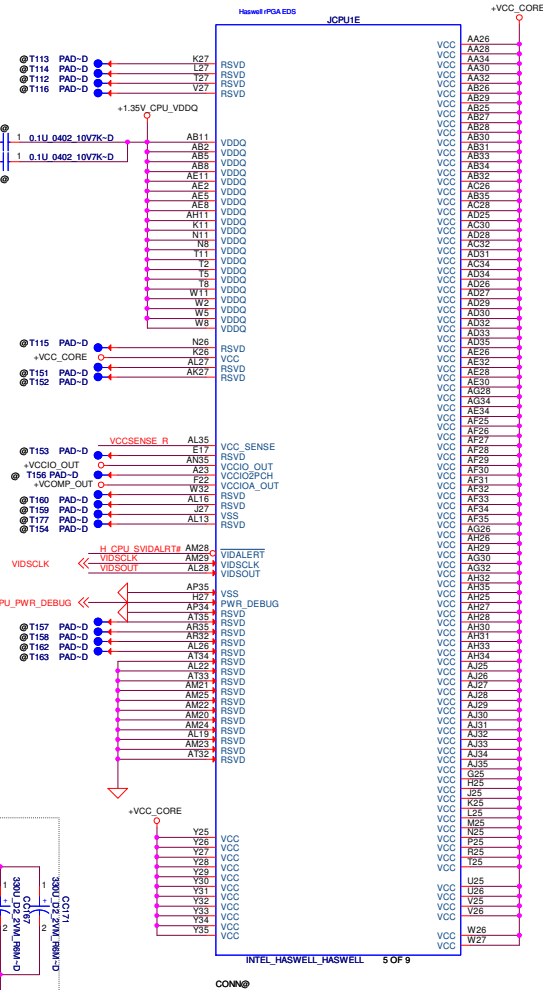
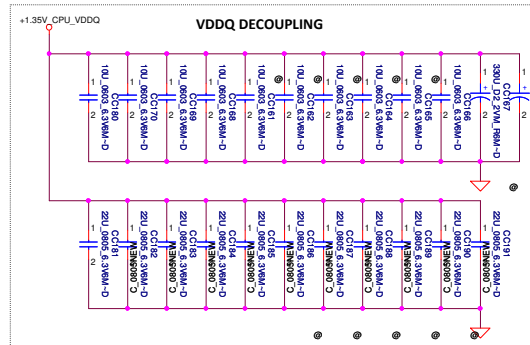
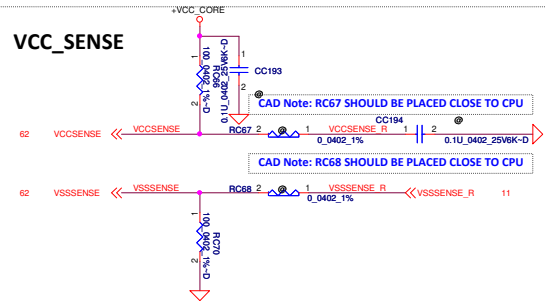
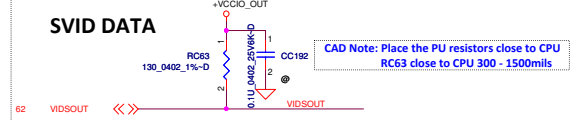
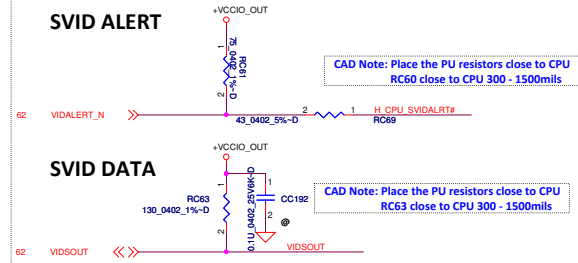
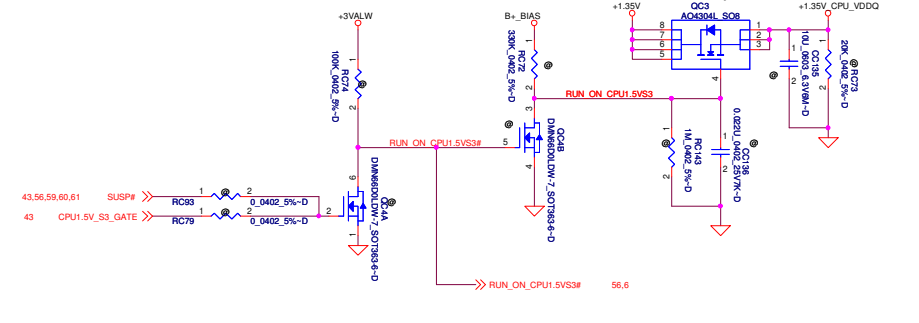


| PCIe Port Bifurcation Straps |  |
|------------------------------|--|
| CFG[6:5]                     | 11: (Default) x16 - Device 1 functions 1 and 2 disabled<br>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled<br>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)<br>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled |

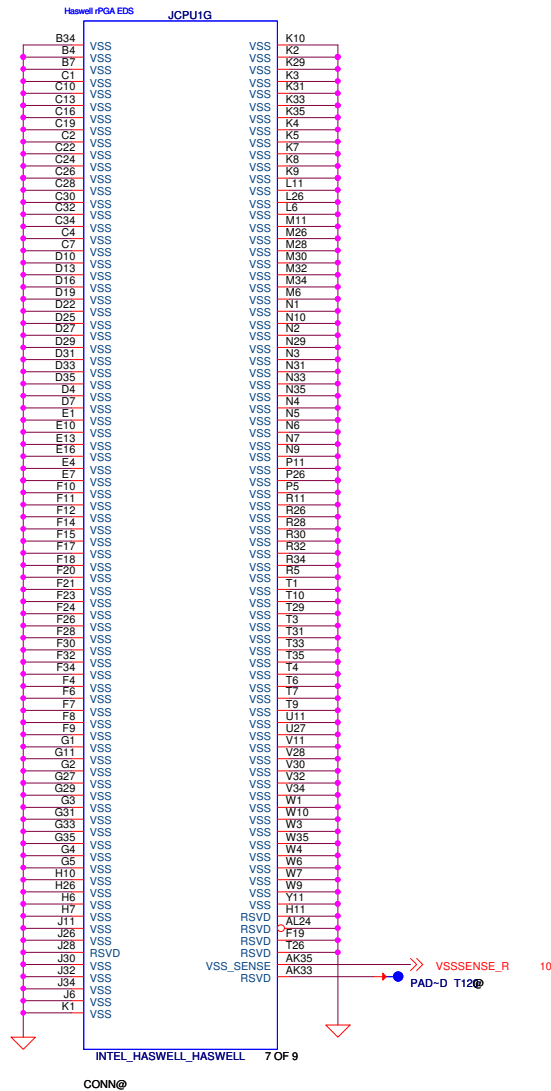
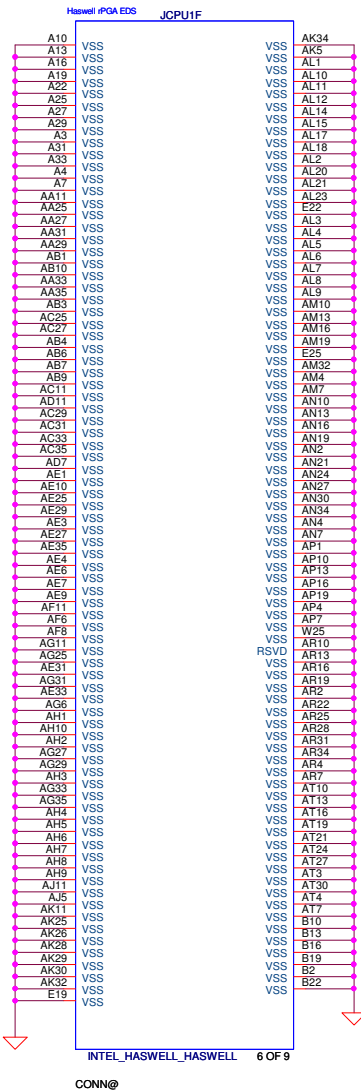


| PEG DEFER TRAINING |   |
|--------------------|---|
| CFG7               | 1: (Default) PEG Train immediately following xxRESETB de assertion<br>0: PEG Wait for BIOS for training |

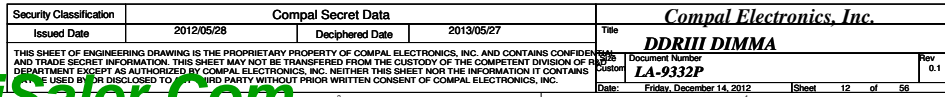


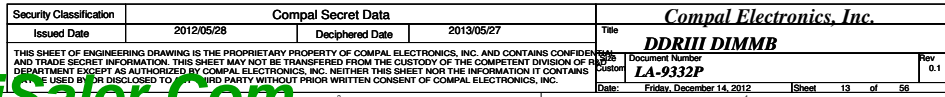


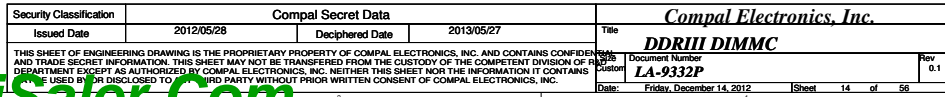
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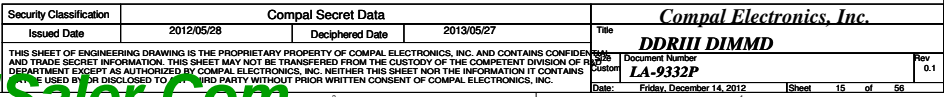


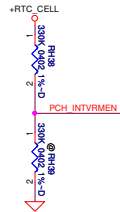
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| CPU (7/7) VSS  |                    |                 |                          | 0.1                             |
| LA-9332P   |                    |                 |                          | Date: Friday, December 14, 2012 |
| Sheet 11 of 56   |                    |                 |                          |                                 |



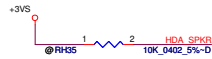




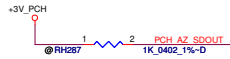




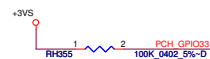
INTVRMEN - INTEGRATED SUS 1.05V VRM  
ENABLE  
High - Enable Internal VRs  
Low - Enable External VRs



NO REBOOT STRAP  
DISABLED WHEN LOW (DEFAULT)  
ENABLED WHEN HIGH



FLASH DESCRIPTOR SECURITY OVERRIDE  
LOW = DISABLED (DEFAULT)  
HIGH = ENABLED

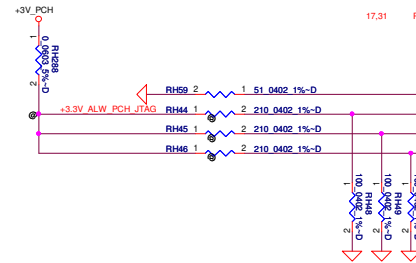
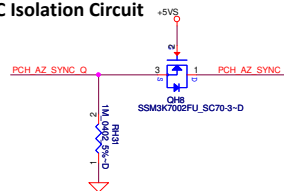


| CMOS_CLR1 | CMOS setting |
|-----------|--------------|
| Shunt     | Clear CMOS   |
| Open      | Keep CMOS    |

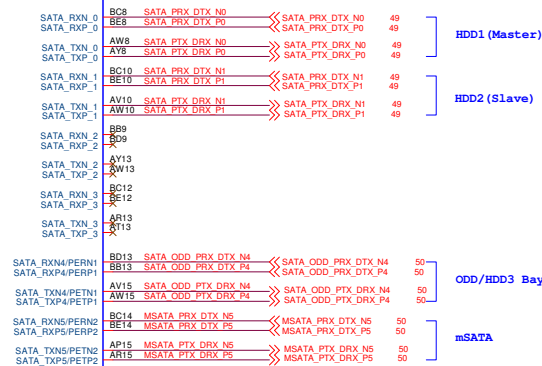
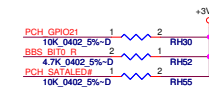
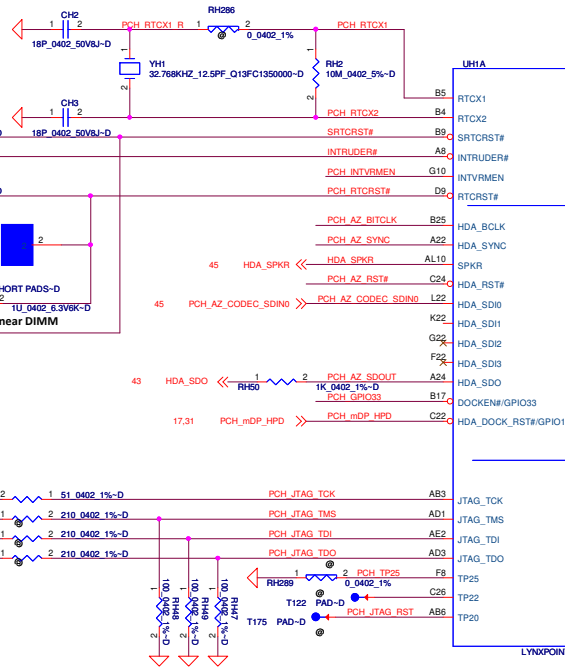
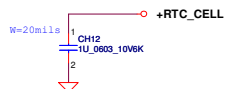
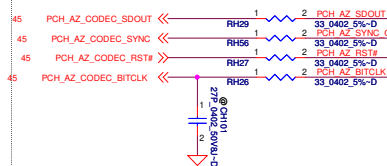
  

| ME_CLR1 | TPM setting            |
|---------|------------------------|
| Shunt   | Clear ME RTC Registers |
| Open    | Keep ME RTC Registers  |

### HDA\_SYNC Isolation Circuit



### HDA for Codec



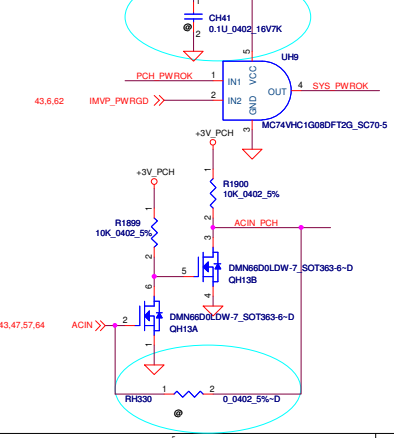
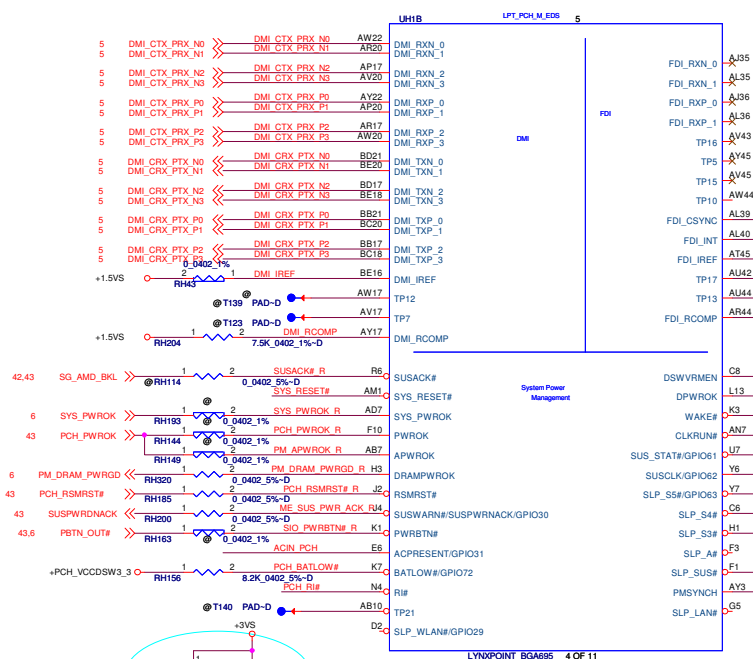
### SATA Impedance Compensation



CAD note:  
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

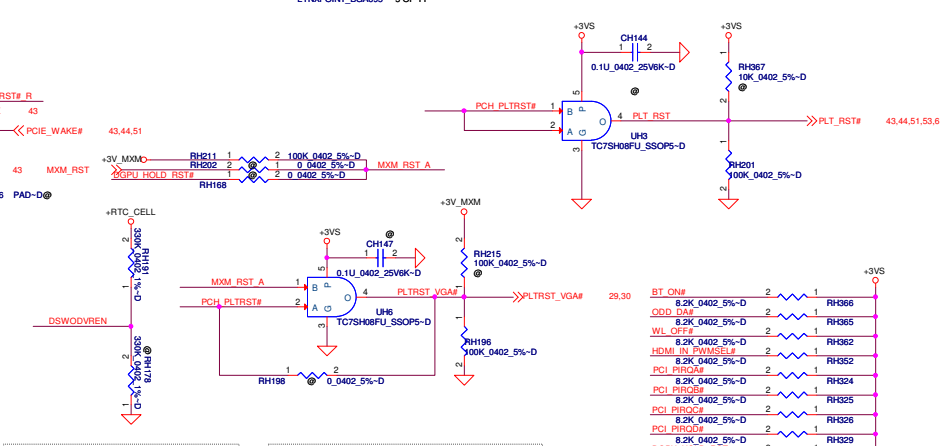
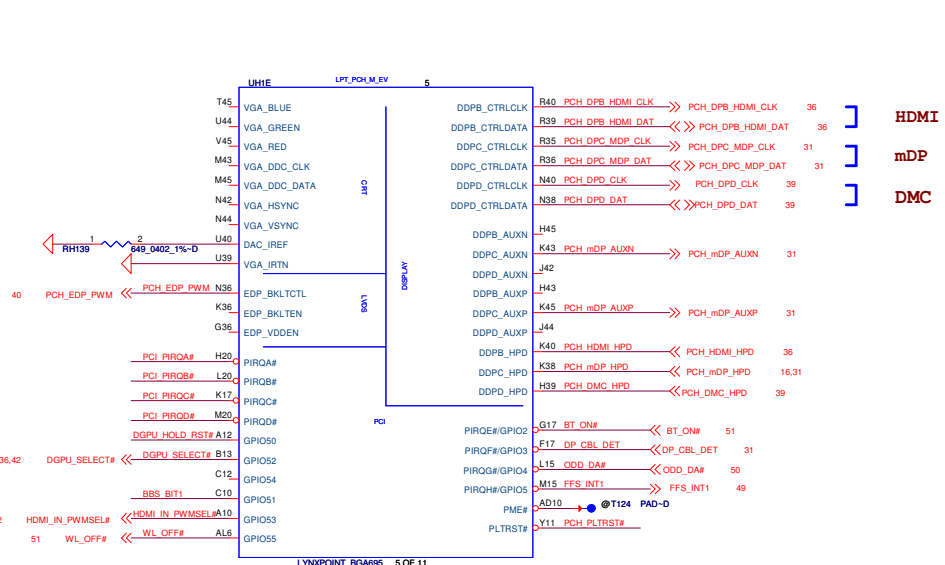
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|--|--------------------|---------------------------------|----------------|
| Issued Date  | 2012/05/28         | LA-9332P                        | 0.1            |
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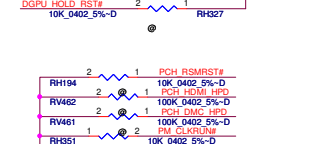
| Boot BIOS Strap         |                            |                    |
|-------------------------|----------------------------|--------------------|
| GNT1#/GPIO15 (BBS_BIT1) | SATA1GP#/GPIO19 (BBS_BIT0) | Boot BIOS Location |
| 0                       | 0                          | LPC                |
| 0                       | 1                          | Reserved (NAND)    |
| 1                       | 0                          | PCI                |
| 1                       | 1                          | SPI                |

GPIO15 has internal pull up.



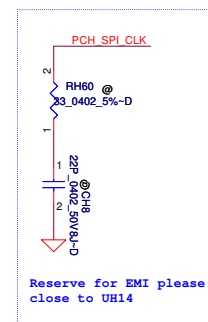
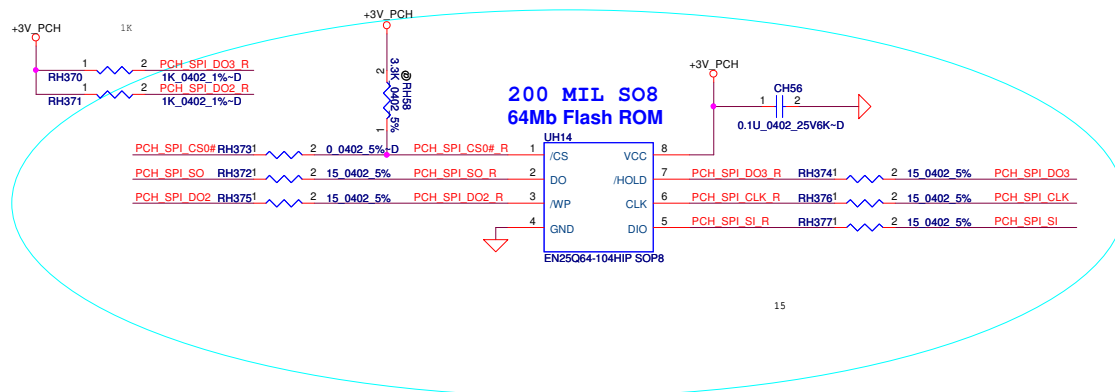
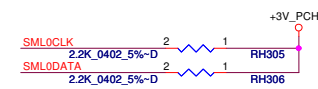
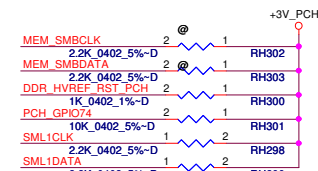
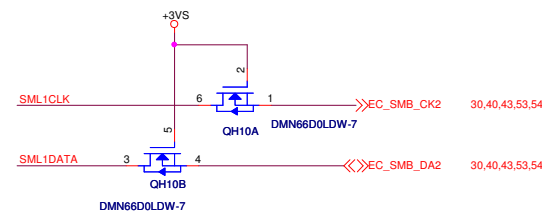
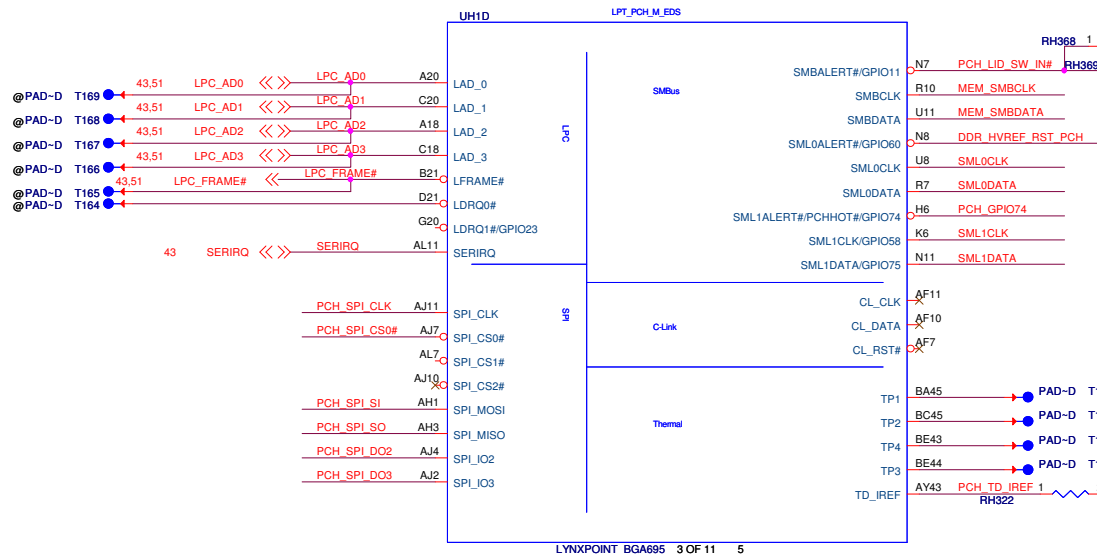
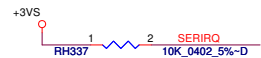
DSWODVREN - ON DIE DSW VR ENABLE  
HIGH = ENABLED (DEFAULT)  
LOW = DISABLED

A16 SWAP OVERRIDE STRAP  
STP\_A16OVR LOW = A16 SWAP OVERRIDE  
HIGH = DEFAULT

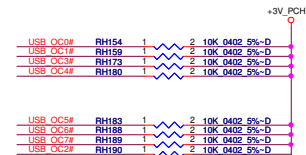




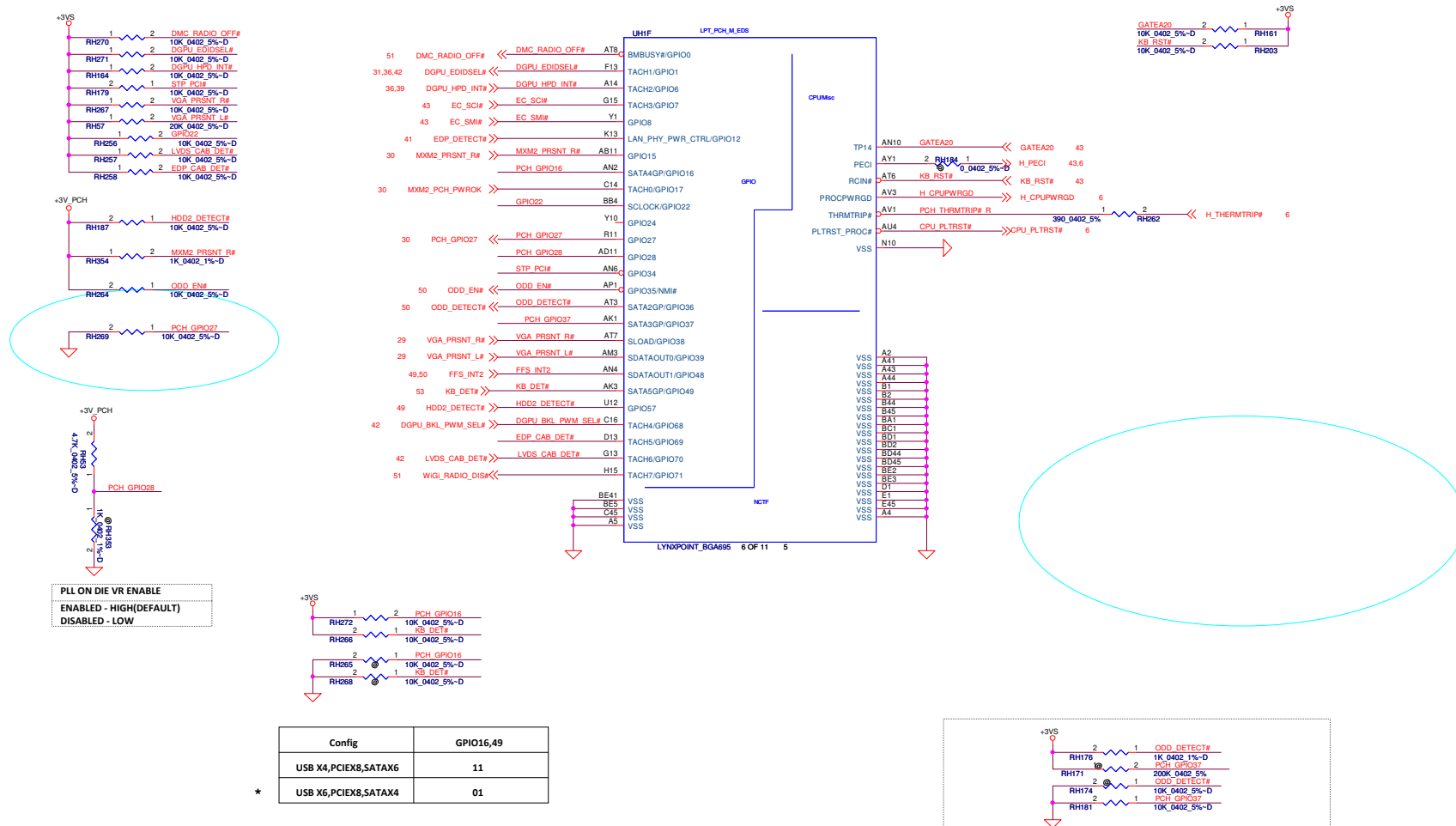
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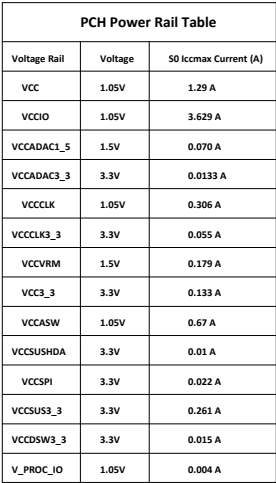
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| Issued Date  | 2012/05/28         | Deciphered Date | 2013/05/27 | PCH (4/9) SPI, SMBUS, LPC |          |
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| Date: Friday, December 14, 2012  |                    |                 |            | Sheet                     | 19 of 56 |



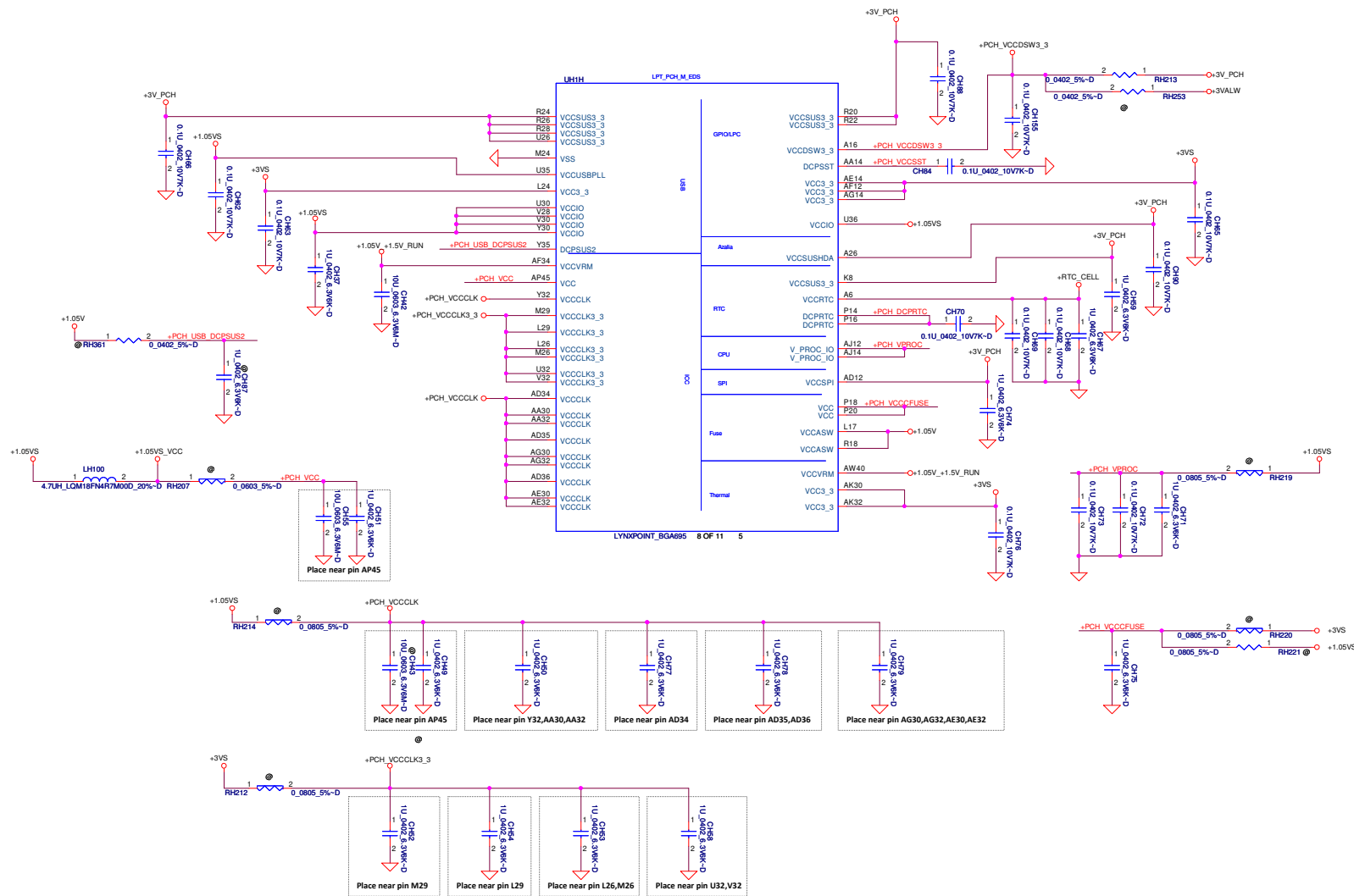
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| Security Classification   |                           | Compal Secret Data |            | Compal Electronics, Inc. |                     |
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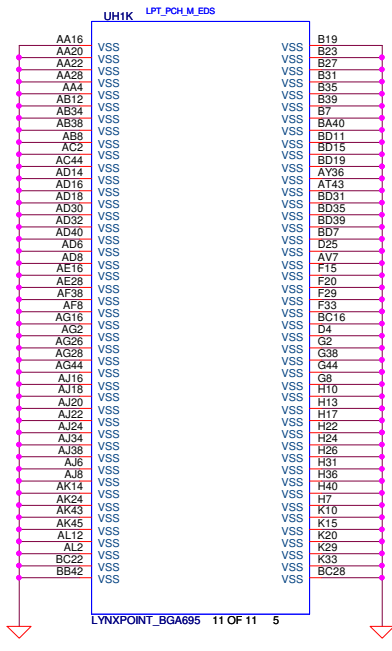
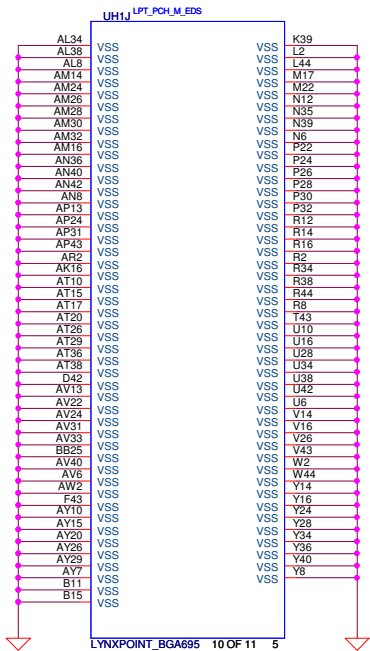
| Fixed Signals |        |        |        | Muxed Signals |        |        |        | Fixed Signals |        |        |        | Muxed Signals |        |        |        | Fixed Signals |        |         |         |
|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|---------|---------|
| USB3_1        | USB3_2 | USB3_5 | USB3_6 | PCIE_1        | PCIE_2 | PCIE_3 | PCIE_4 | PCIE_5        | PCIE_6 | PCIE_7 | PCIE_8 | SATA_4        | SATA_5 | SATA_6 | SATA_7 | SATA_8        | SATA_9 | SATA_10 | SATA_11 |
|               |        |        |        | (00)          | (00)   |        |        |               |        |        |        | (00)          | (00)   |        |        |               |        |         |         |
|               |        |        |        | USB3_3        | USB3_4 |        |        |               |        |        |        | PCIE_1        | PCIE_2 |        |        |               |        |         |         |
|               |        |        |        | (01)          | (01)   |        |        |               |        |        |        | (01)          | (01)   |        |        |               |        |         |         |



| PCH Power Rail Table |         |                       |
|----------------------|---------|-----------------------|
| Voltage Rail         | Voltage | S0 Iccmax Current (A) |
| VCC                  | 1.05V   | 1.29 A                |
| VCCIO                | 1.05V   | 3.629 A               |
| VCCADAC1_5           | 1.5V    | 0.070 A               |
| VCCADAC3_3           | 3.3V    | 0.0133 A              |
| VCCCLK               | 1.05V   | 0.306 A               |
| VCCCLK3_3            | 3.3V    | 0.055 A               |
| VCCVRM               | 1.5V    | 0.179 A               |
| VCC3_3               | 3.3V    | 0.133 A               |
| VCCASW               | 1.05V   | 0.67 A                |
| VCCSUSHDA            | 3.3V    | 0.01 A                |
| VCCSPI               | 3.3V    | 0.022 A               |
| VCCSUS3_3            | 3.3V    | 0.261 A               |
| VCCDSW3_3            | 3.3V    | 0.015 A               |
| V_PROC_IO            | 1.05V   | 0.004 A               |



|  |                    |                 |                          |                                 |
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|  |                    |                 |                          | Rev 0.1                         |



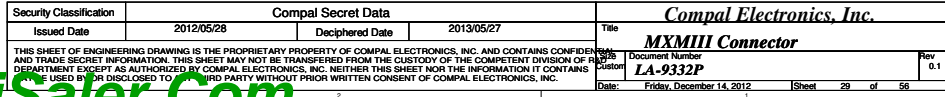


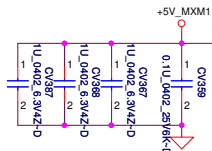
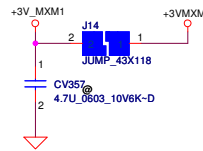
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|  |                    |                 |            | Date: Friday, December 14, 2012 | Rev<br>0.1                  |
|  |                    |                 |            | Sheet 25 of 56                  |                             |

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|  |            |                    |            | Sheet                    | 27 of 56                    |
|  |            |                    |            | Rev                      | 0.1                         |

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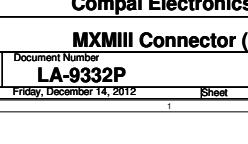
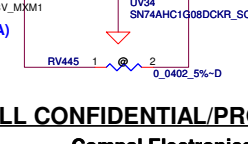
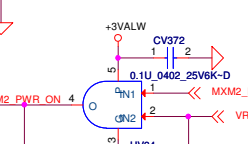
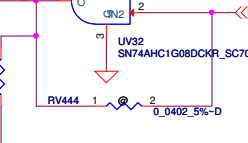
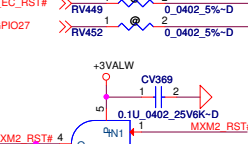
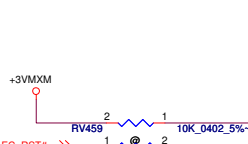
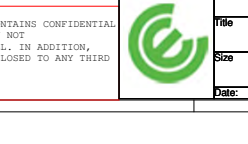
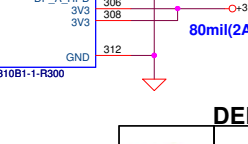
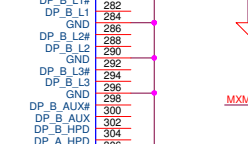
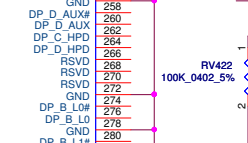
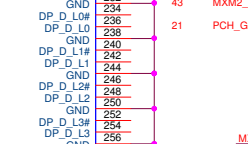
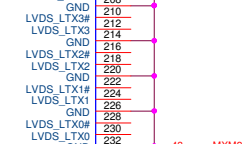
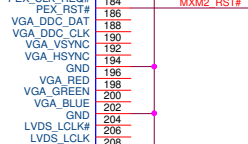
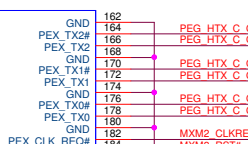
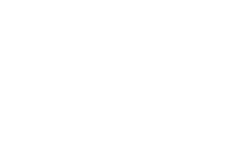
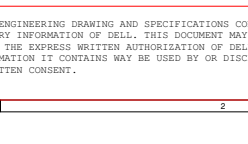
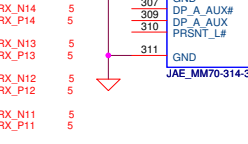
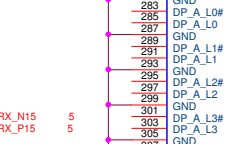
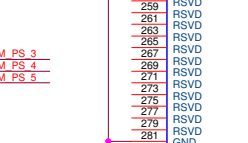
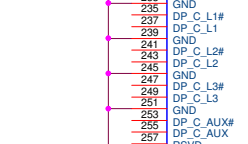
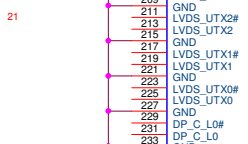
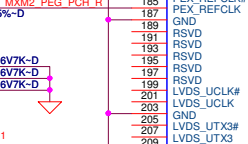
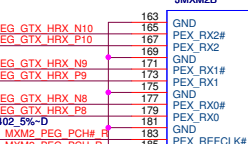
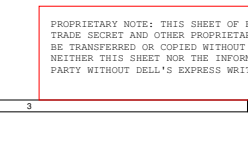
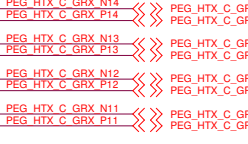
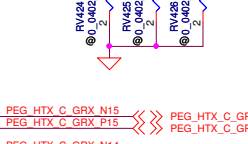
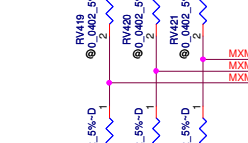
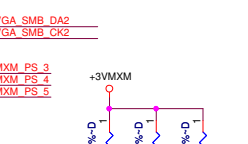
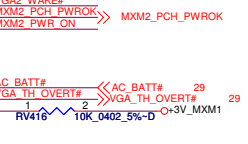
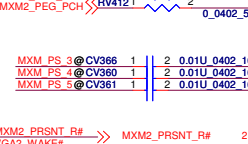
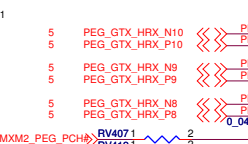
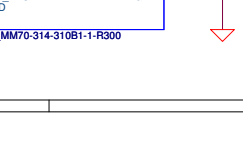
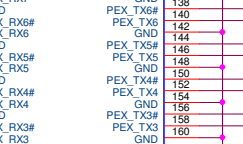
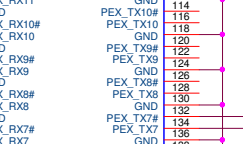
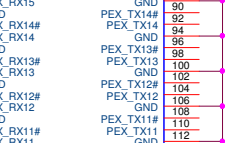
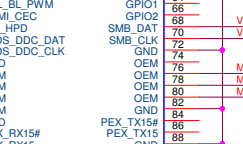
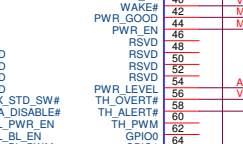
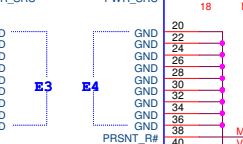
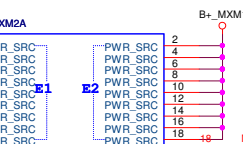
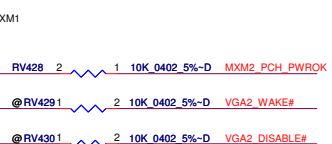
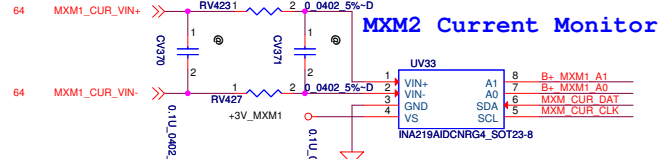
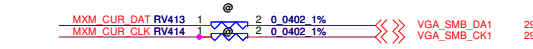
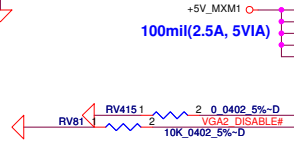
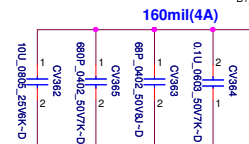
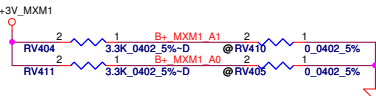




02/21-109

04/06-118

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Compal Electronics, Inc.

MXMIII Connector (Slave)

LA-9332P

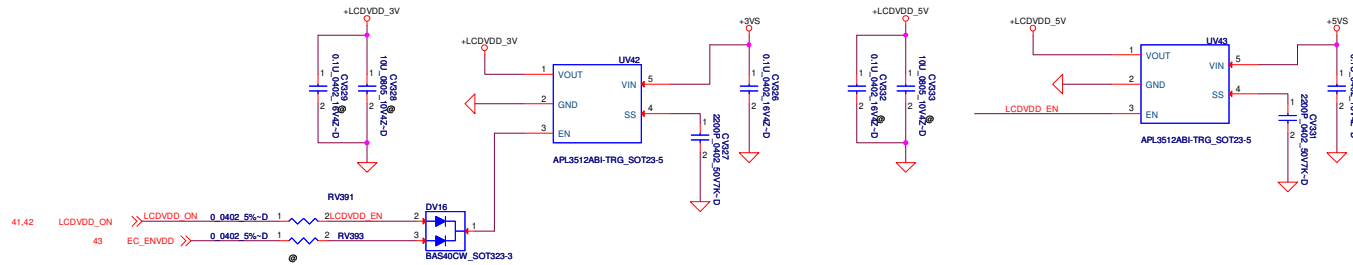
Friday, December 14, 2012



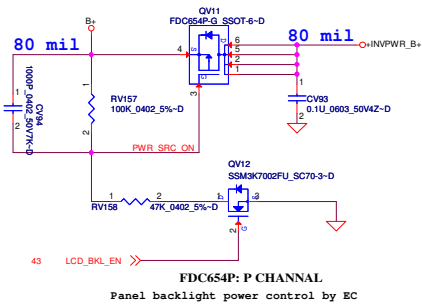
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| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc.        |                  |
| Issued Date   | 2012/05/14         | Deciphered Date | 2013/05/13 | Title                           | eDP SW-CPU & MXM |
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|   |                    |                 |            | LA-9332P                        | 0.1              |
|   |                    |                 |            | Date: Friday, December 14, 2012 | Sheet 32 of 56   |



## LCD POWER

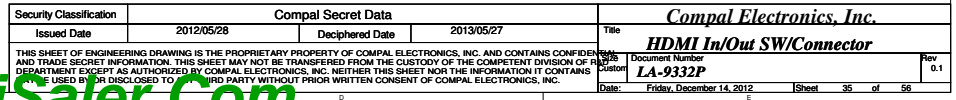


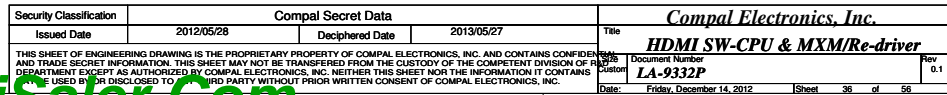
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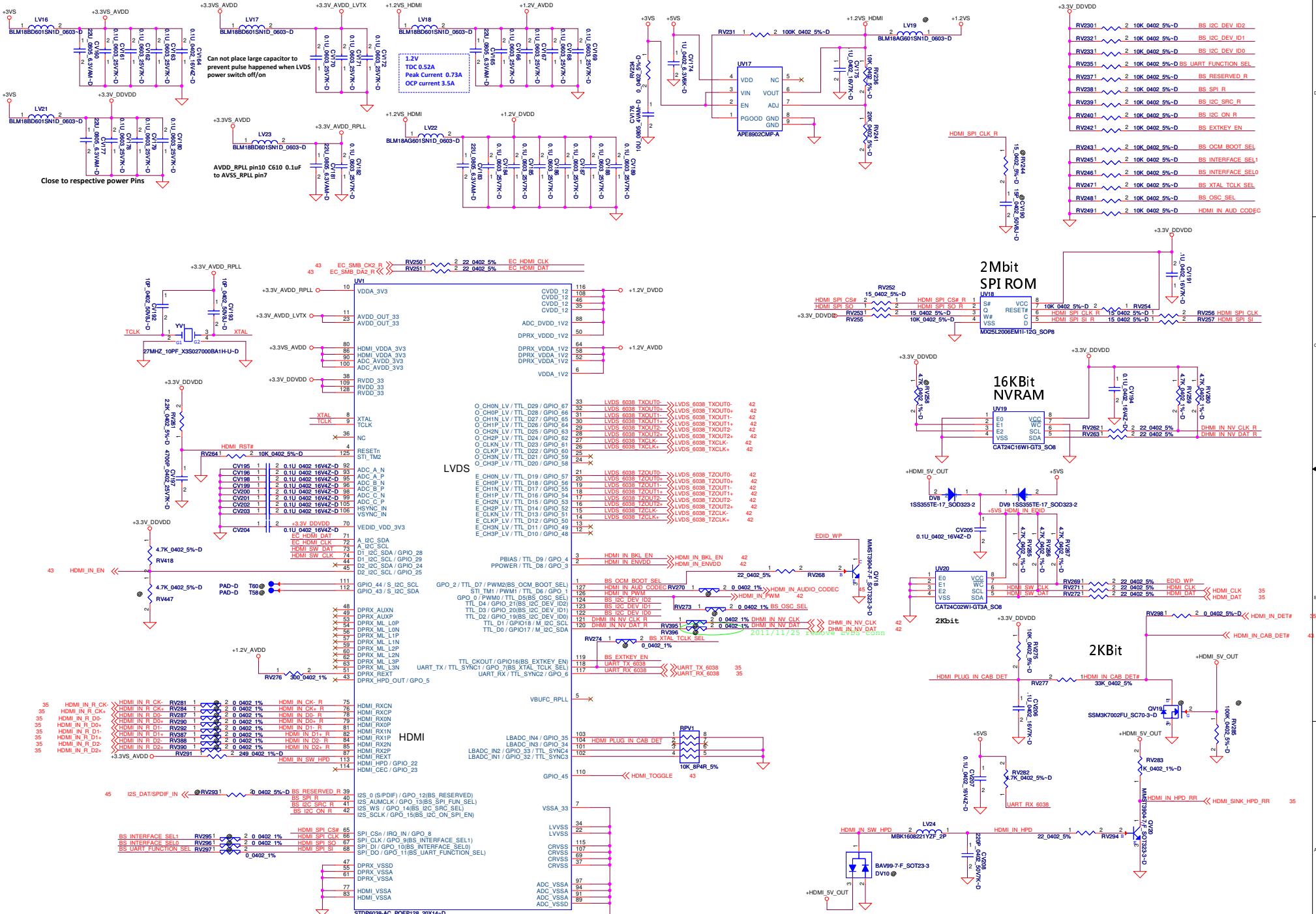


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|  |            |                           |            | LA-9332P                 | 0.1      |
| Date:  |            | Friday, December 14, 2012 |            | Sheet                    | 33 of 56 |

|   |                    |                 |            |                                 |                |
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| Issued Date   | 2012/05/14         | Deciphered Date | 2013/05/13 | <i>reserved</i>                 |                |
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|   |                    |                 |            | LA-9332P                        | 0.1            |
|   |                    |                 |            | Date: Friday, December 14, 2012 | Sheet 34 of 56 |

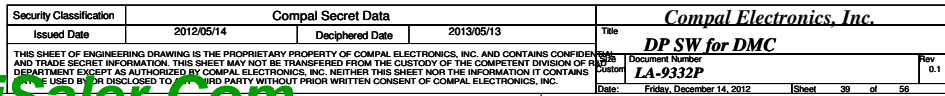






| Security Classification   |  | Compal Secret Data |  | Compal Electronics, Inc. |  |
|---|--|--------------------|--|--------------------------|--|
| Issued Date   |  | Deciphered Date    |  | Title                    |  |
| 2012/05/14  |  | 2013/05/13         |  | HDMI to LVDS-STD P6038   |  |
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| Date: Friday, December 14, 2012   |  | Sheet              |  | 37 of 56                 |  |

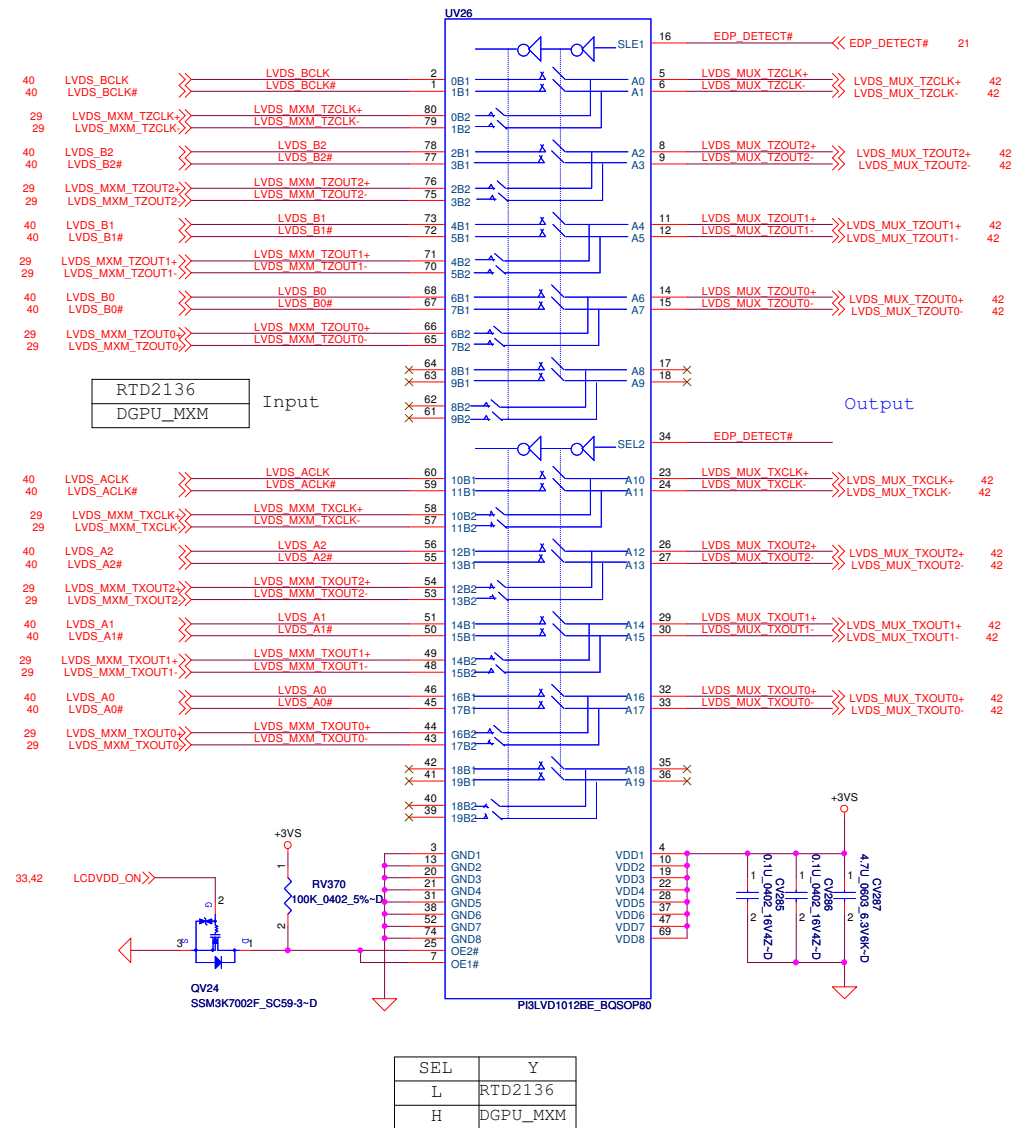
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| Issued Date   | 2012/05/14         | Deciphered Date | 2013/05/13 | Title                    | LVDS to eDP-STDP4028      |
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|   |                    |                 |            | Date                     | Friday, December 14, 2012 |
|   |                    |                 |            | Sheet                    | 38 of 58                  |
|   |                    |                 |            | Rev                      | 0.1                       |

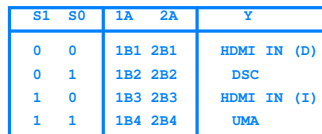




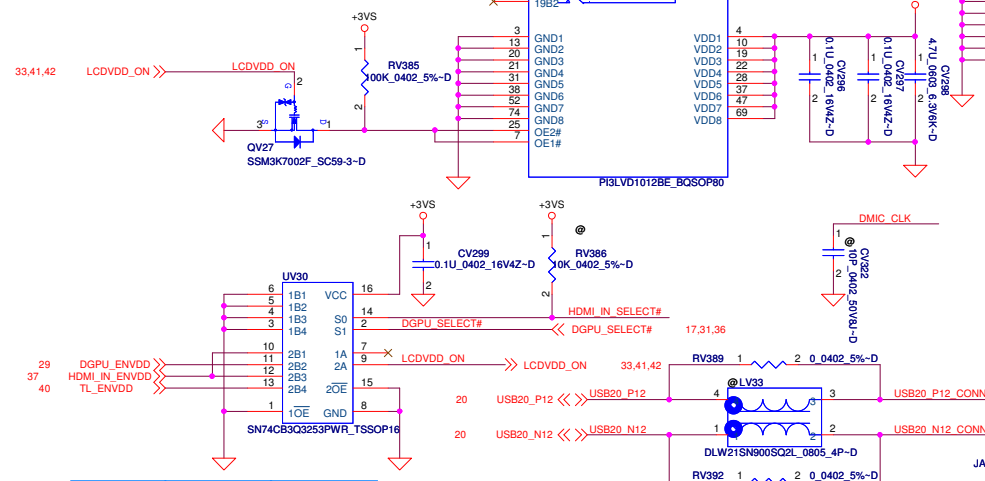


## STDP6038 SW STDP4028 PCH/GPU AUX for LVDS





| S1 | S0 | 1A  | 2A  | Y           |
|----|----|-----|-----|-------------|
| 0  | 0  | 1B1 | 2B1 | HDMI IN (D) |
| 0  | 1  | 1B2 | 2B2 | DSC         |
| 1  | 0  | 1B3 | 2B3 | HDMI IN (I) |
| 1  | 1  | 1B4 | 2B4 | UMA         |

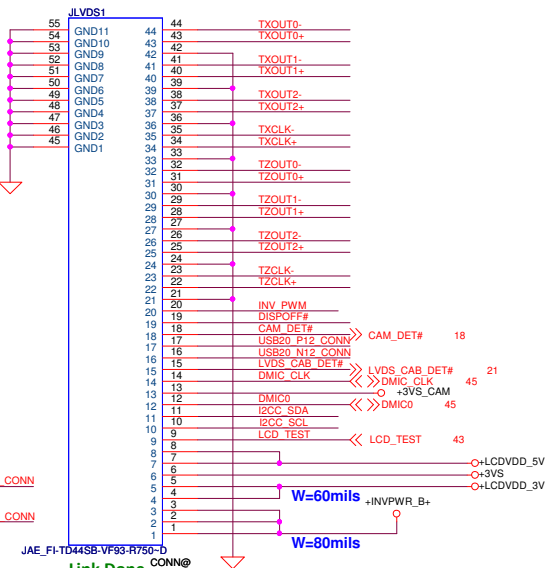
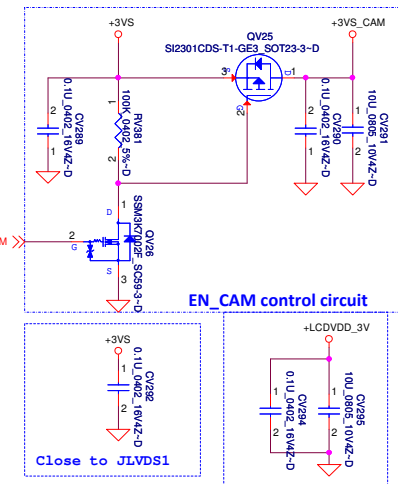


| S1 | S0 | 1A  | 2A  | Y       |
|----|----|-----|-----|---------|
| 0  | 0  | 1B1 | 2B1 | HDMI IN |
| 0  | 1  | 1B2 | 2B2 | DSC     |
| 1  | 0  | 1B3 | 2B3 | HDMI IN |
| 1  | 1  | 1B4 | 2B4 | UMA     |



|     |    |
|-----|----|
| SEL | Y  |
| L   | B1 |
| H   | B2 |

JLVDS1

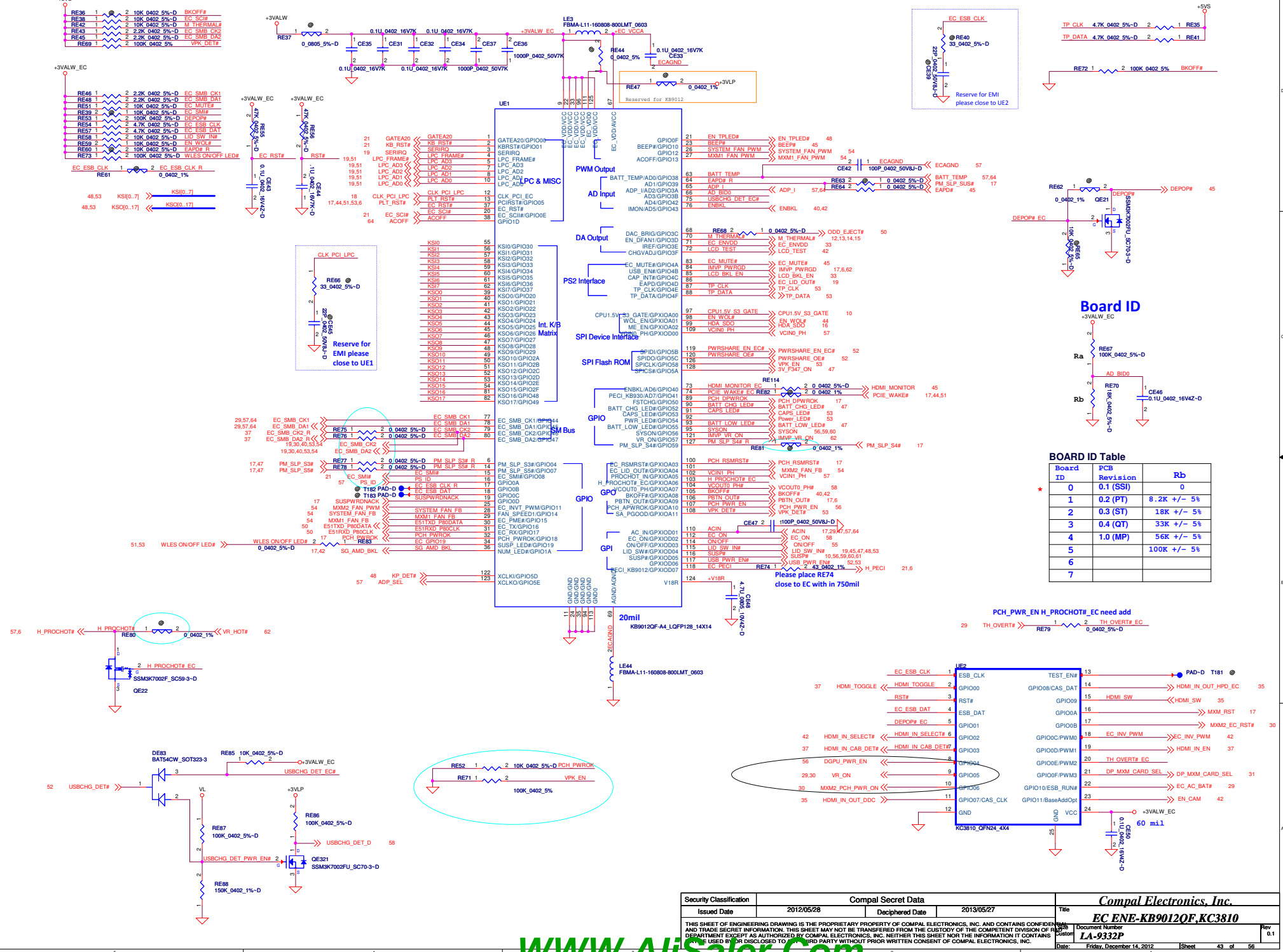


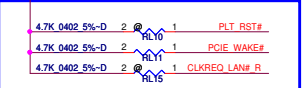
**DELL CONFIDENTIAL/PROPRIETARY**

**LVDS SW- 6038/SYSTEM & CONN**

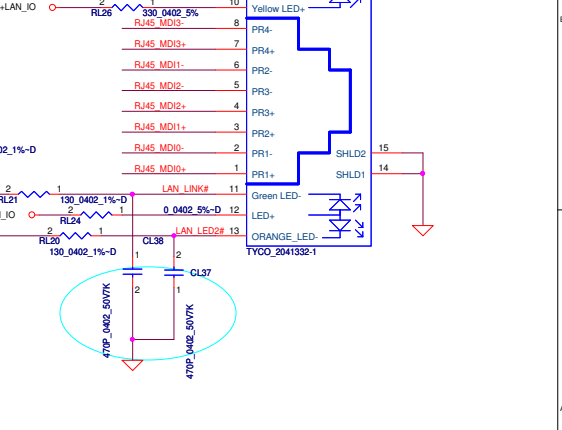
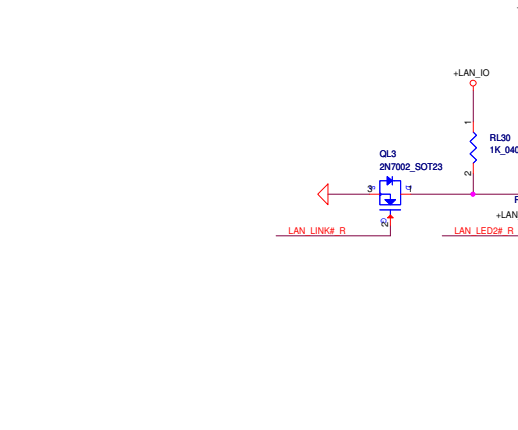
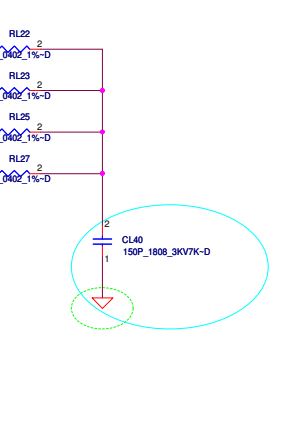
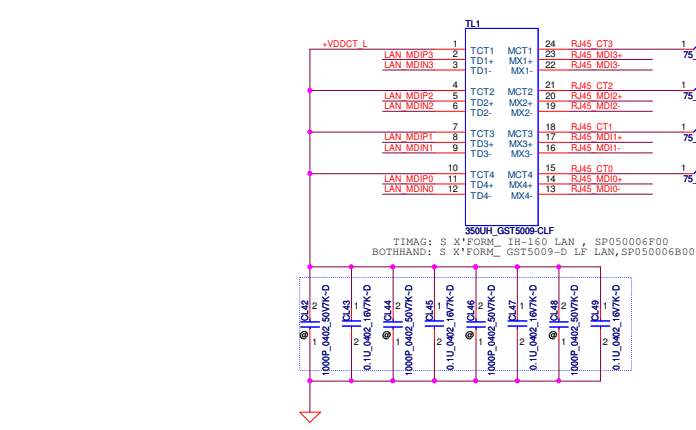
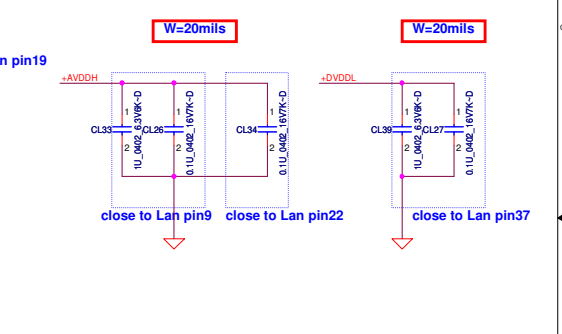
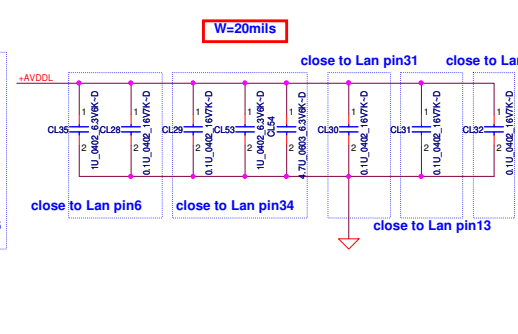
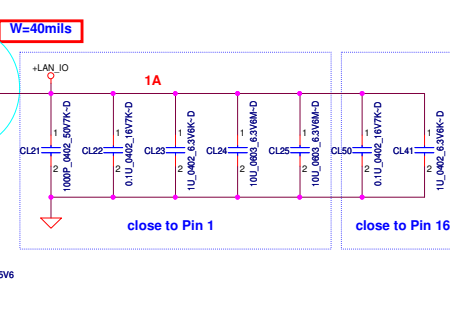
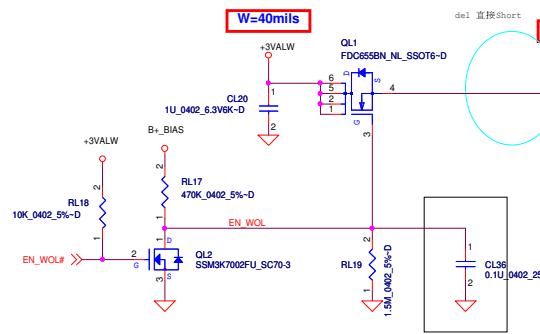
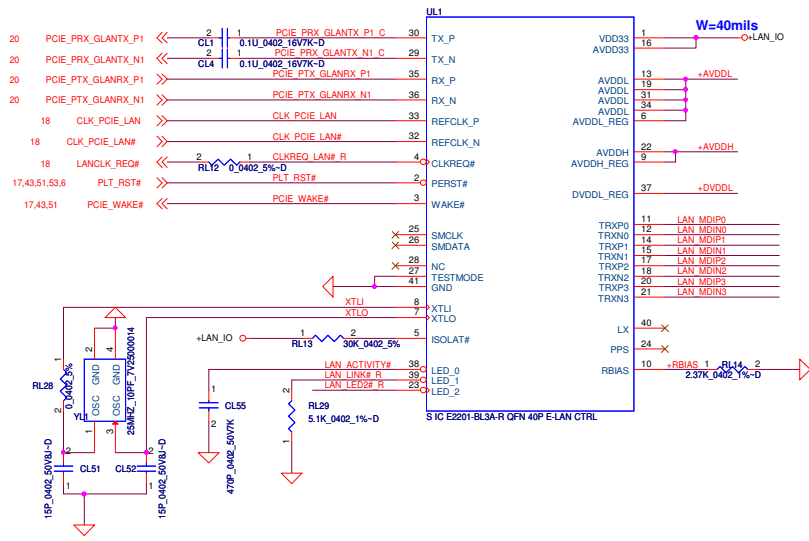
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|-------|---------------------------|----------------|
| Size  | Document Number           | Rev            |
|       | <b>LA-9332P</b>           | 0.1            |
| Date: | Friday, December 14, 2012 | Sheet 42 of 56 |

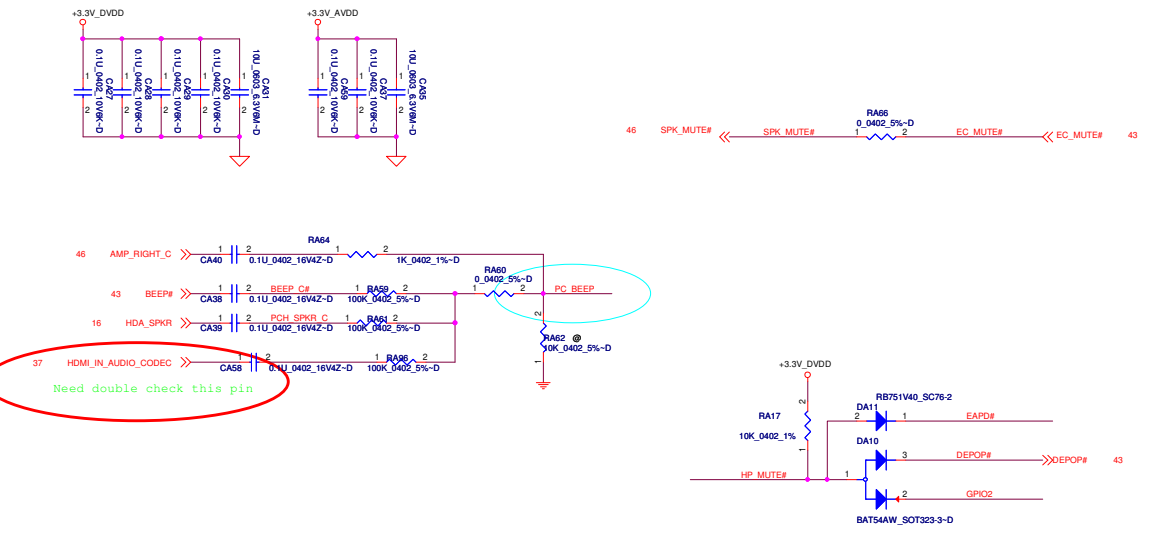
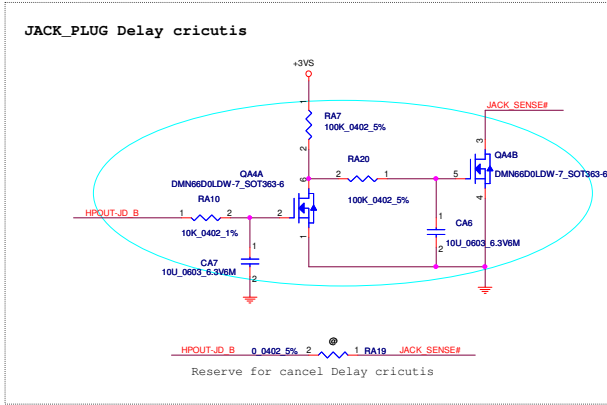
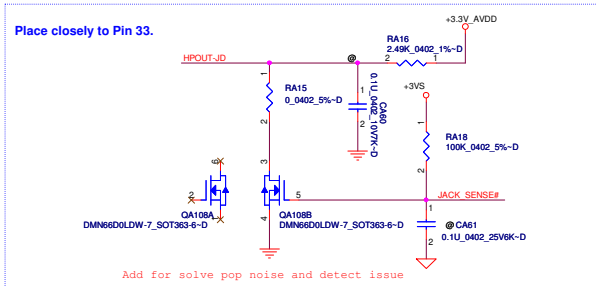
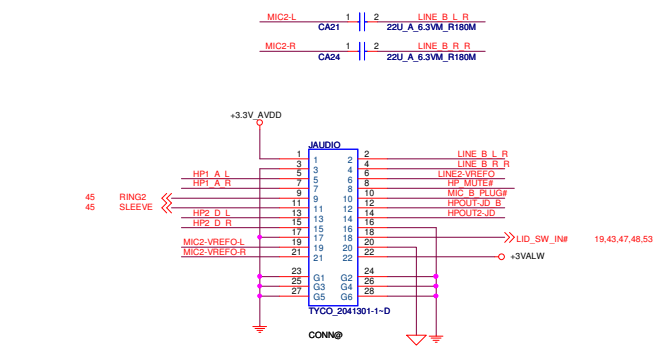
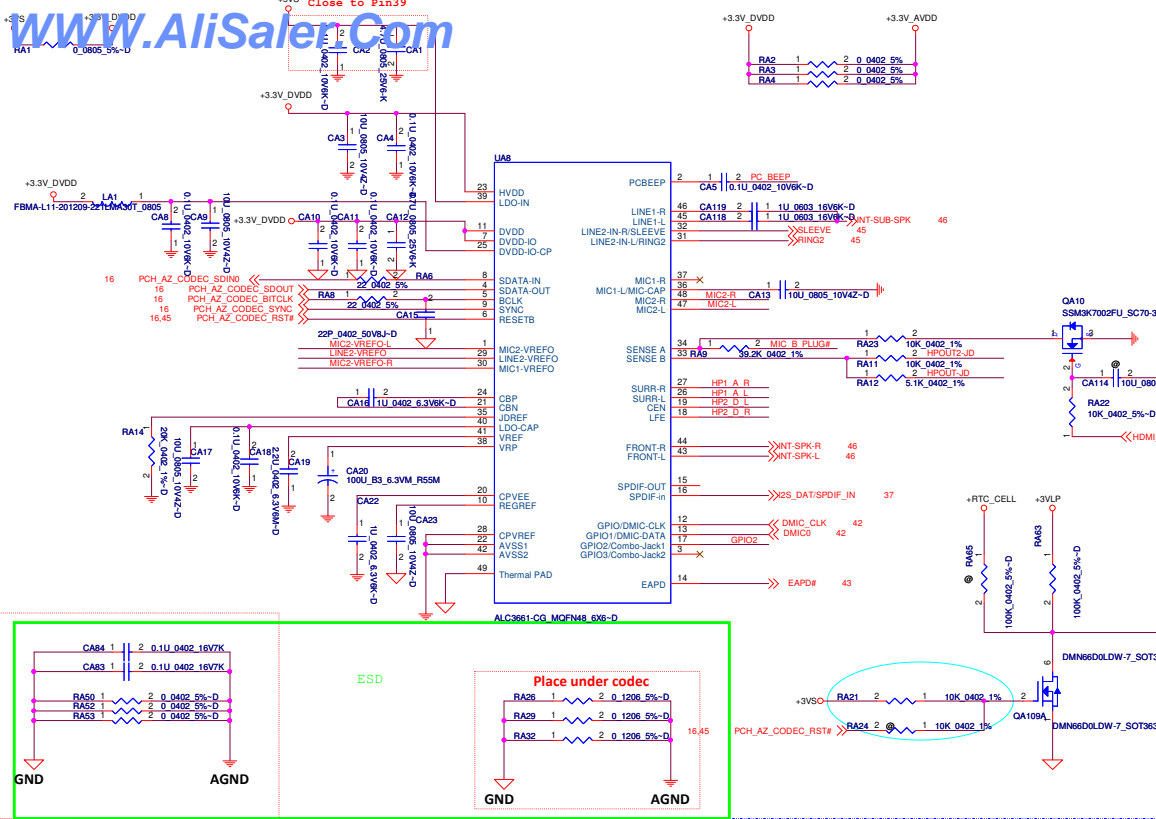
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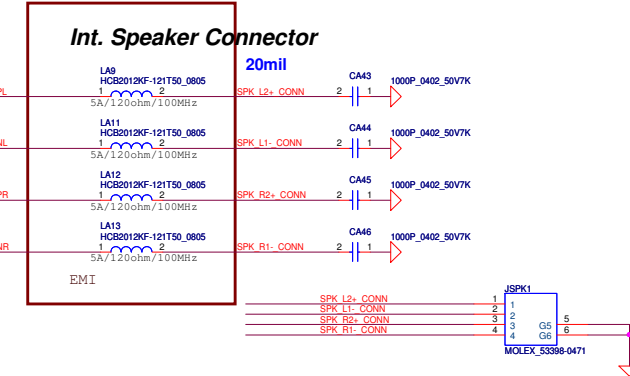
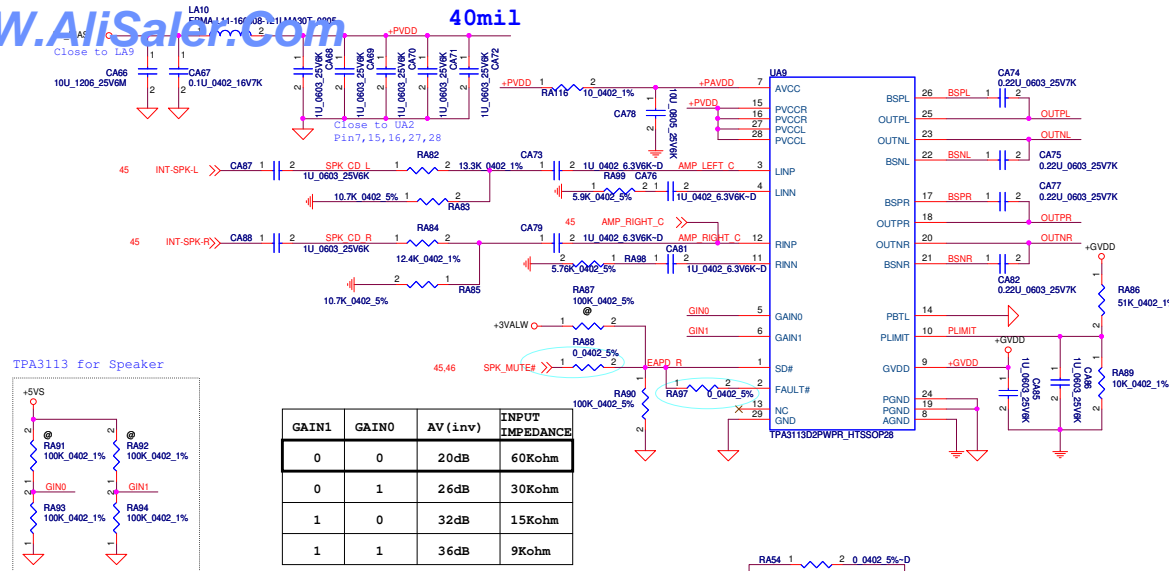




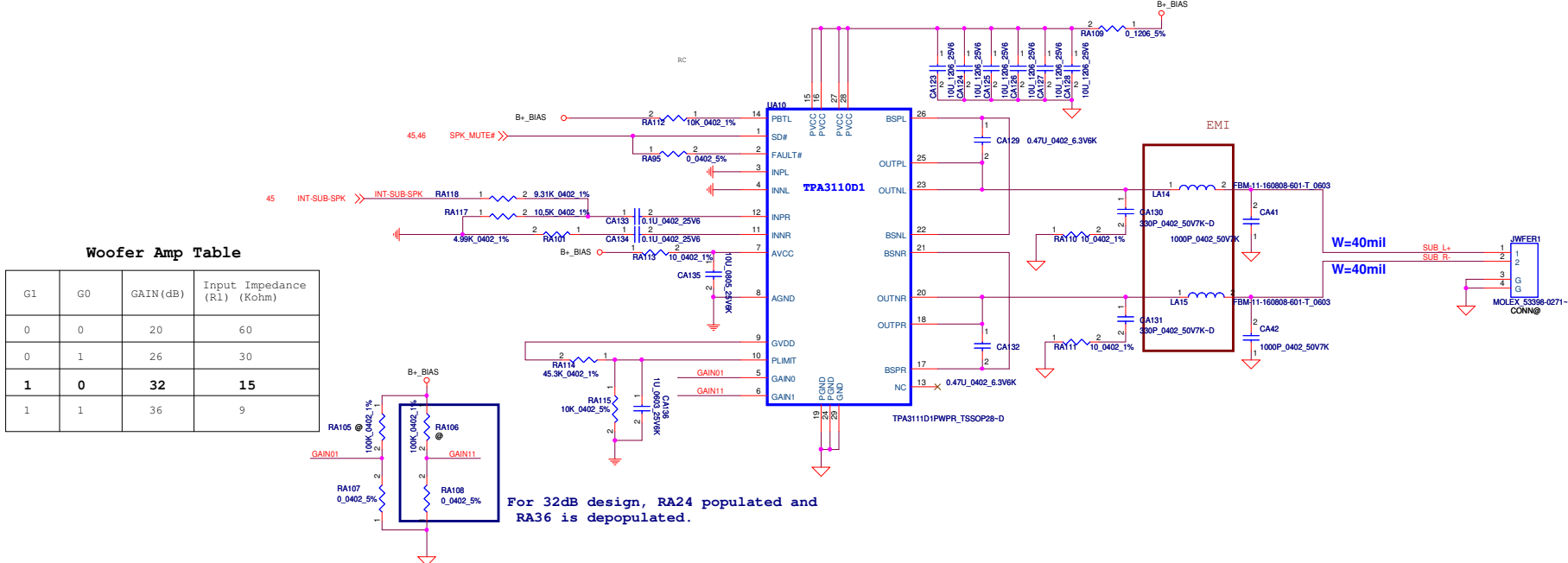
The pull-up resistors might not be necessary due to existence on PCH side.

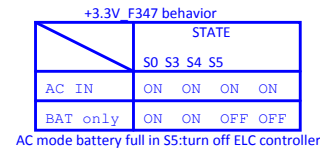
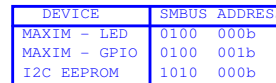






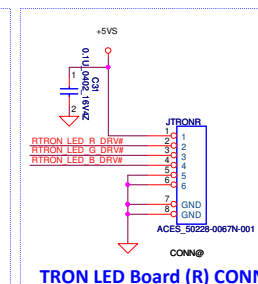
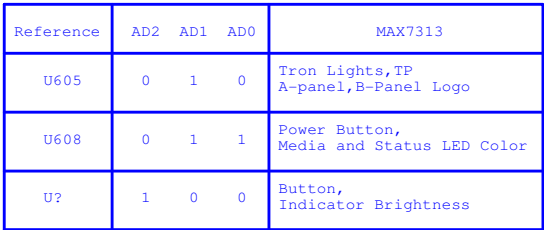
Speaker amp impedance of JBL is 4 ohm.



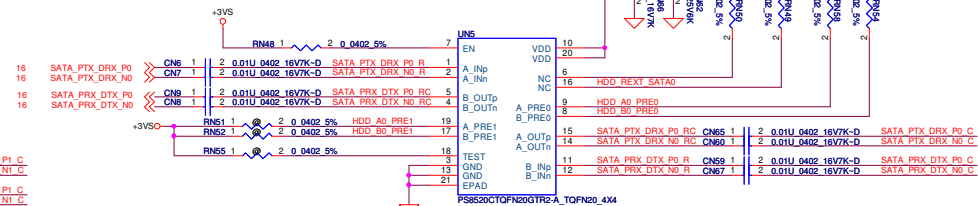
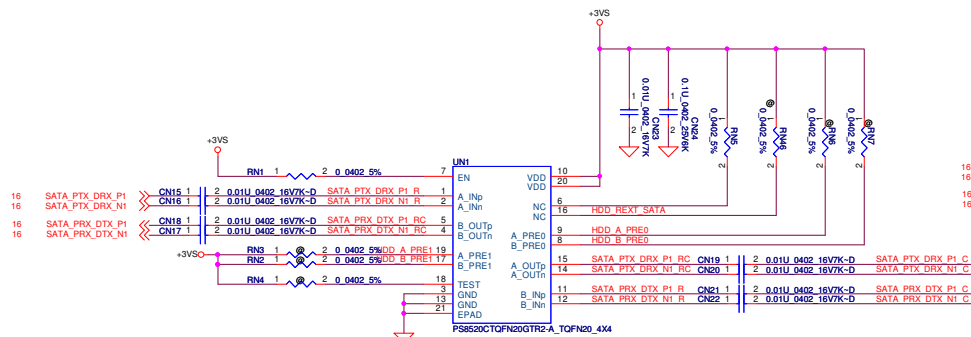
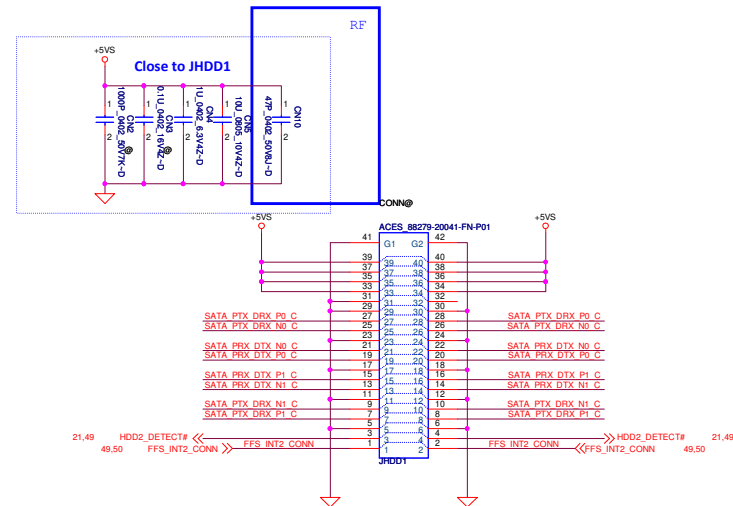
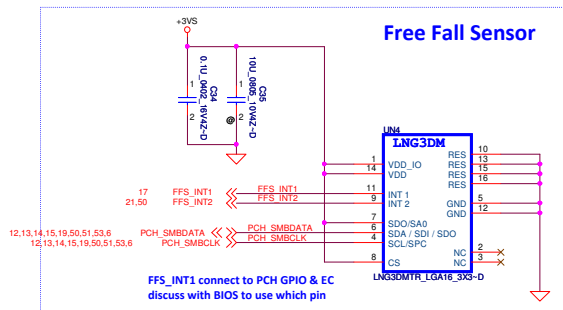


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|  |                    |                 |            | Date                     | LA-9332P                  | 0.1            |
|  |                    |                 |            | Issue                    | Friday, December 14, 2012 | Sheet 47 of 56 |









Pin 20:  
PARADE PS8250B:  
Reserve RN12  
PERICOM P13EQX6741ST:  
Mount RN46, Reserve RN12  
ASMEDIA ASM1466:  
Mount RN46, Reserve RN12

Pin 9:  
PARADE PS8250B:  
Reserve RN11  
PERICOM P13EQX6741ST:  
Reserve RN11  
ASMEDIA ASM1466:  
Mount RN11 to pull down

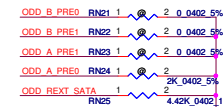
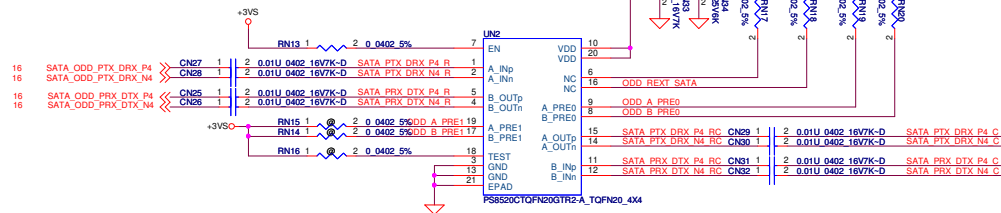
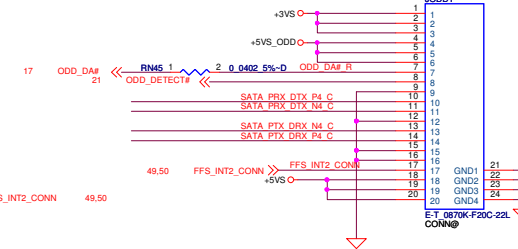
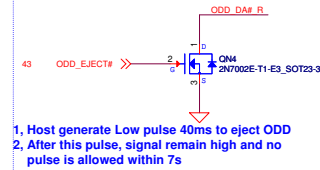
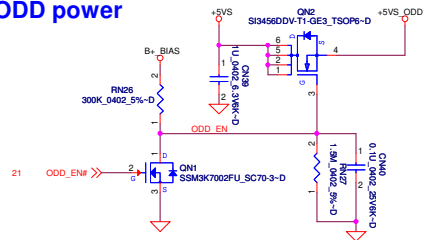
HDD\_B\_PREG0 RN8 1 2 0.0402 5%  
HDD\_B\_PREG1 RN8 1 2 0.0402 5%  
HDD\_A\_PREG1 RN10 1 2 0.0402 5%  
HDD\_A\_PREG0 RN11 1 2 0.0402 5%  
HDD\_REXT SATA RN12 1 2 5.1K 0.402 1%

Pin 20:  
PARADE PS8250B:  
Reserve RN49, Mount RN57  
PERICOM P13EQX6741ST:  
Mount RN49, Reserve RN57  
ASMEDIA ASM1466:  
Mount RN49, Reserve RN57

Pin 9:  
PARADE PS8250B:  
Reserve RN29  
PERICOM P13EQX6741ST:  
Reserve RN29  
ASMEDIA ASM1466:  
Mount RN29 to pull down

HDD\_B\_PREG0 RN3 1 2 0.0402 5%  
HDD\_B\_PREG1 RN6 1 2 0.0402 5%  
HDD\_A\_PREG1 RN7 1 2 0.0402 5%  
HDD\_A\_PREG0 RN9 1 2 0.0402 5%  
HDD\_REXT SATA RN57 1 2 5.1K 0.402 1%

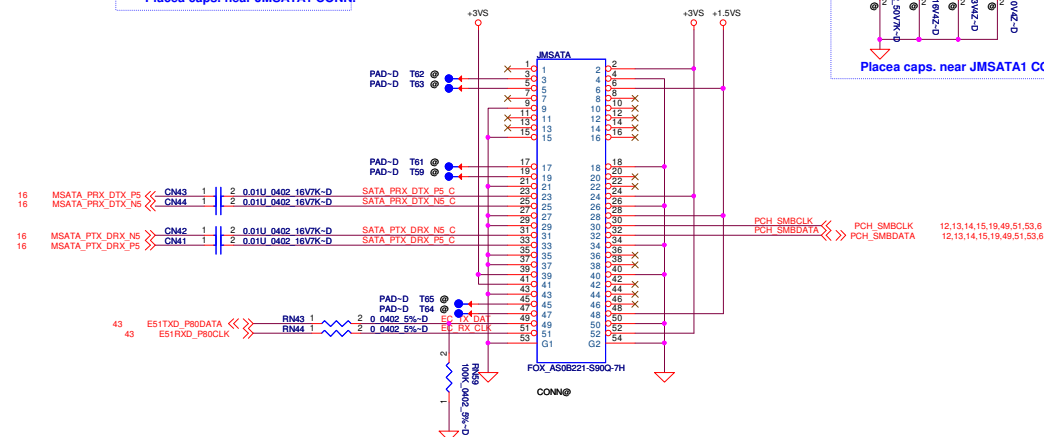
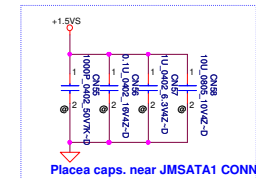
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| Security Classification  | Compal Secret Data |                 |            | Compal Electronics, Inc. |
| Issued Date  | 2012/05/28         | Deciphered Date | 2013/05/27 | Document Number          |
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| Date: Friday, December 14, 2012  |                    |                 |            | Sheet 49 of 56           |



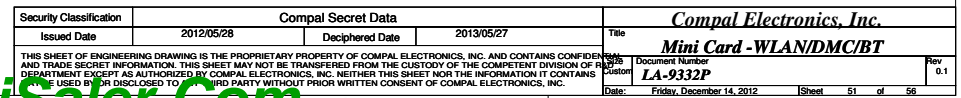
Pin 9:  
PARADE PS8250B:  
Reserve RN24.

PERICOM PI3EQX6741ST:  
Reserve RN24

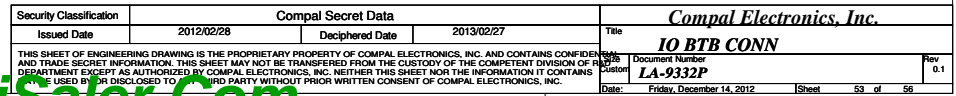
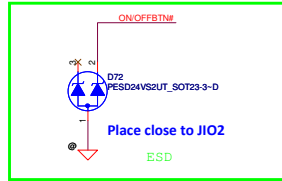
ASMEDIA ASM1466:  
Mount RN24 to pull down



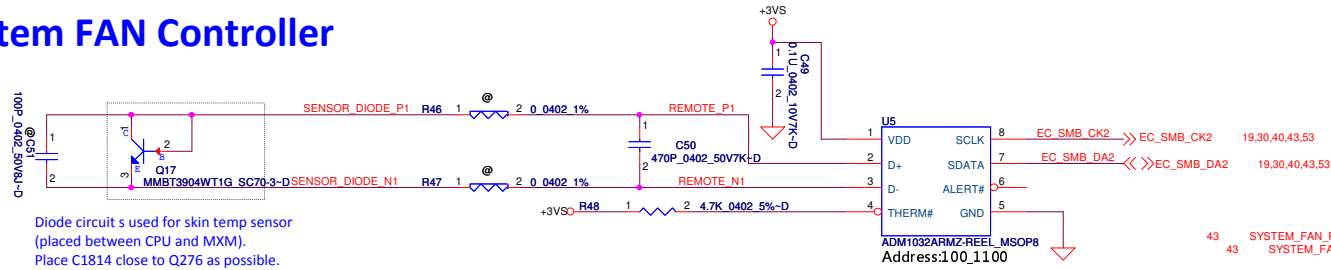
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|--|--------------------|-----------------|-------------------------------------|--|
| Security Classification  | Compul Secret Data |                 | Title                               |  |
| Issued Date  | 2012/05/28         | Deciphered Date | 2013/05/27                          | <i>Compul Electronics, Inc.</i><br><b>SATA ODD/mSATA</b> |
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|  |                    |                 | <b>LA-932P</b>                      | <b>0.1</b>   |
|  |                    |                 | Date: <b>Fri, December 14, 2012</b> | Sheet 50 of 56   |





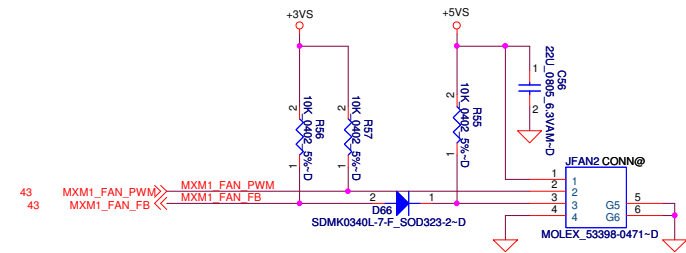
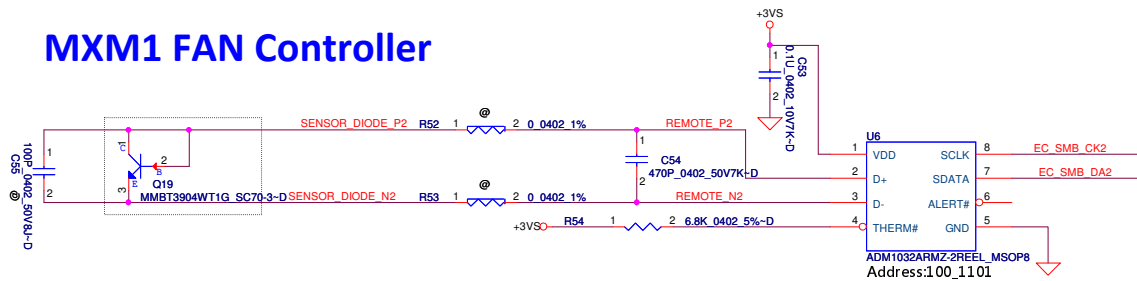


## System FAN Controller

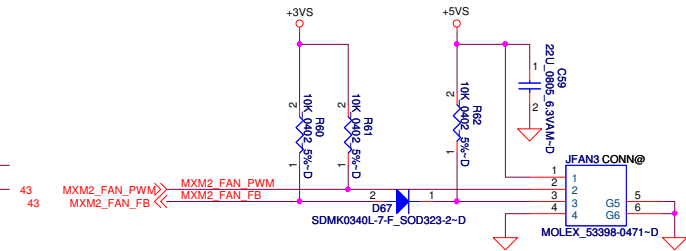
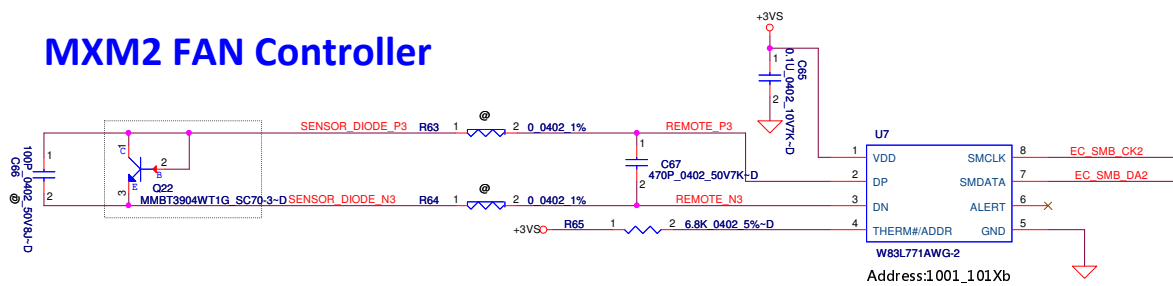


| Pull up resistor<br>on thermtrip pin | SMBUS address |
|--------------------------------------|---------------|
| 4.7k                                 | 1111          |
| 6.8k                                 | 1011          |
| 10k                                  | 1001          |
| 15k                                  | 1101          |
| 22k                                  | 0011          |
| 33k                                  | 0111          |

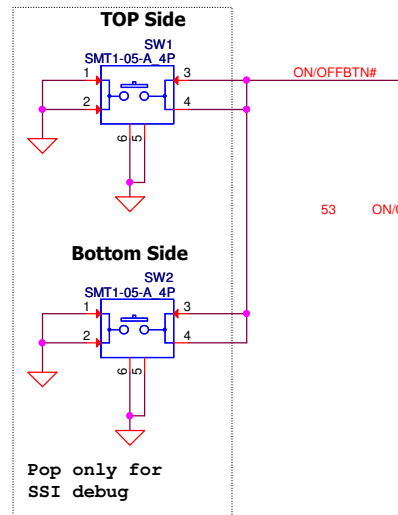
## MXM1 FAN Controller



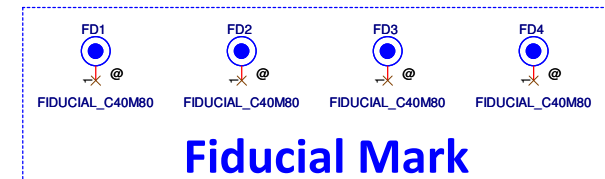
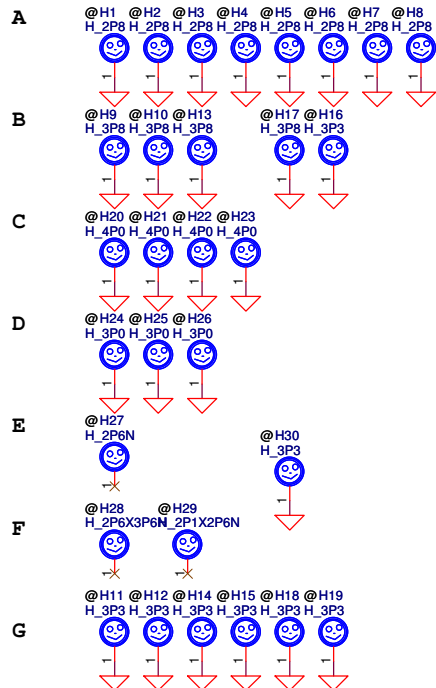
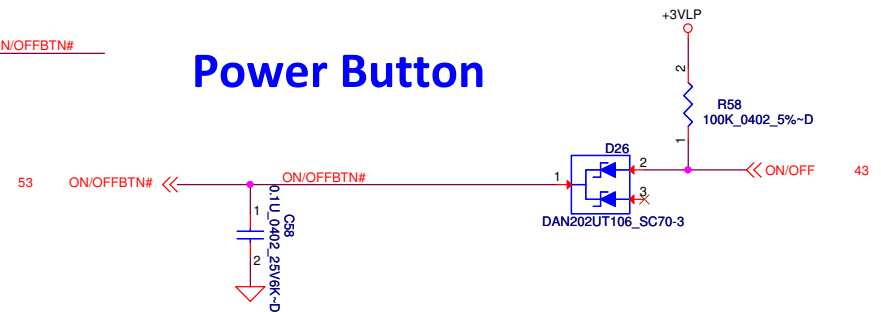
## MXM2 FAN Controller



# ON/OFF switch

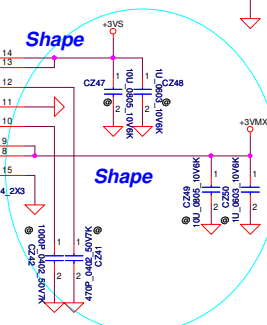
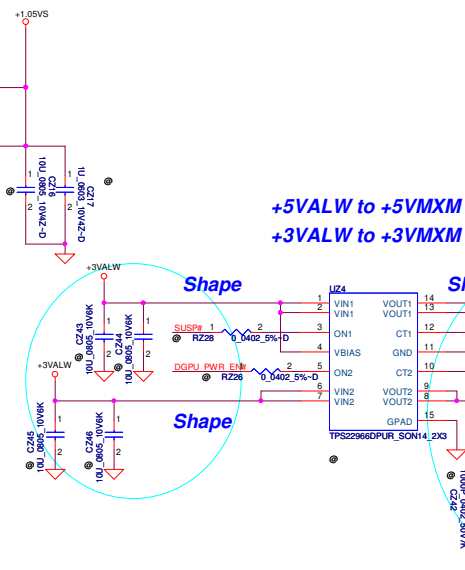
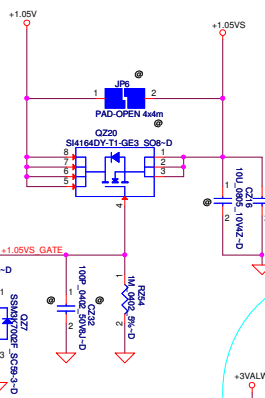
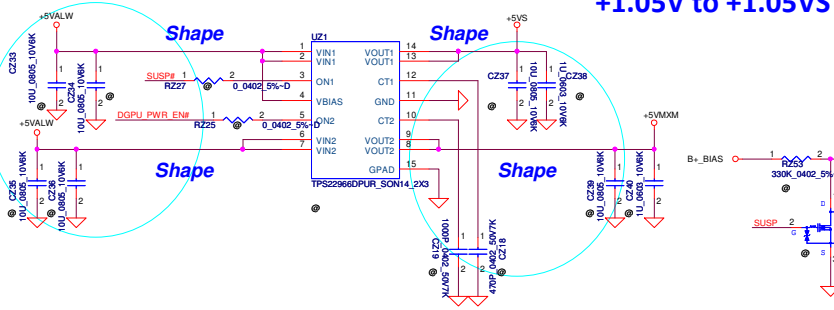
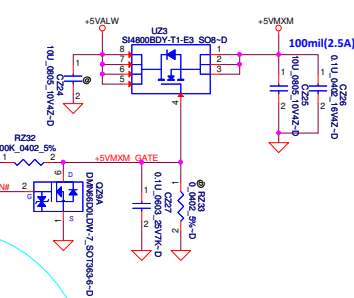
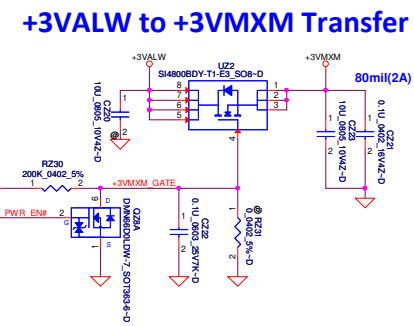
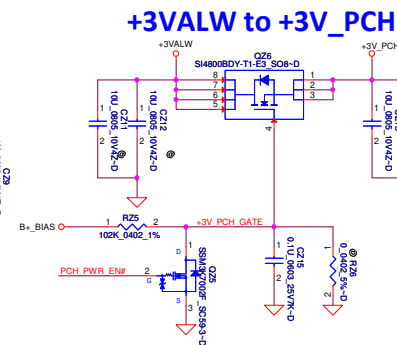
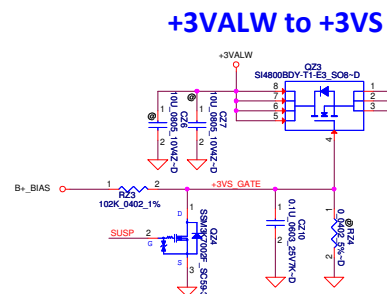
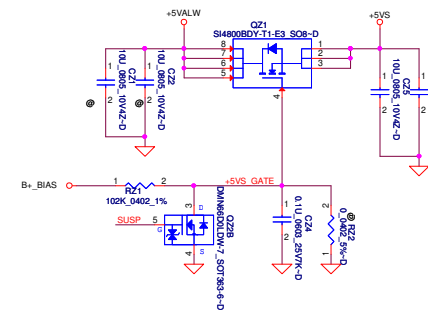


# Power Button

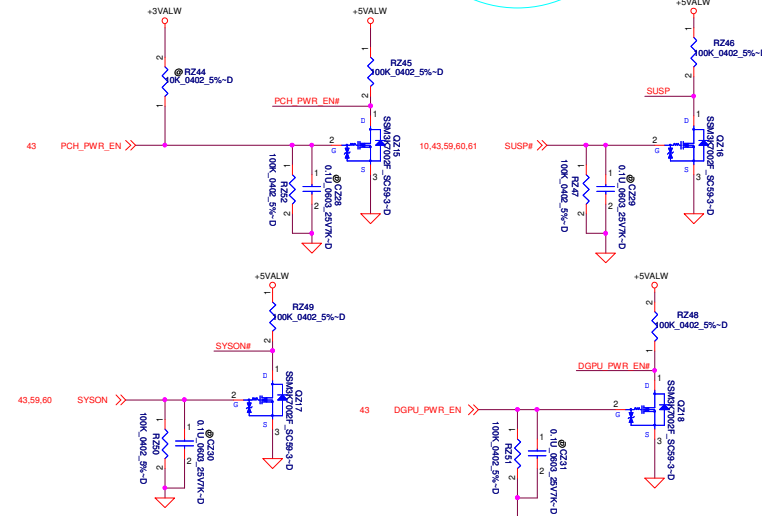
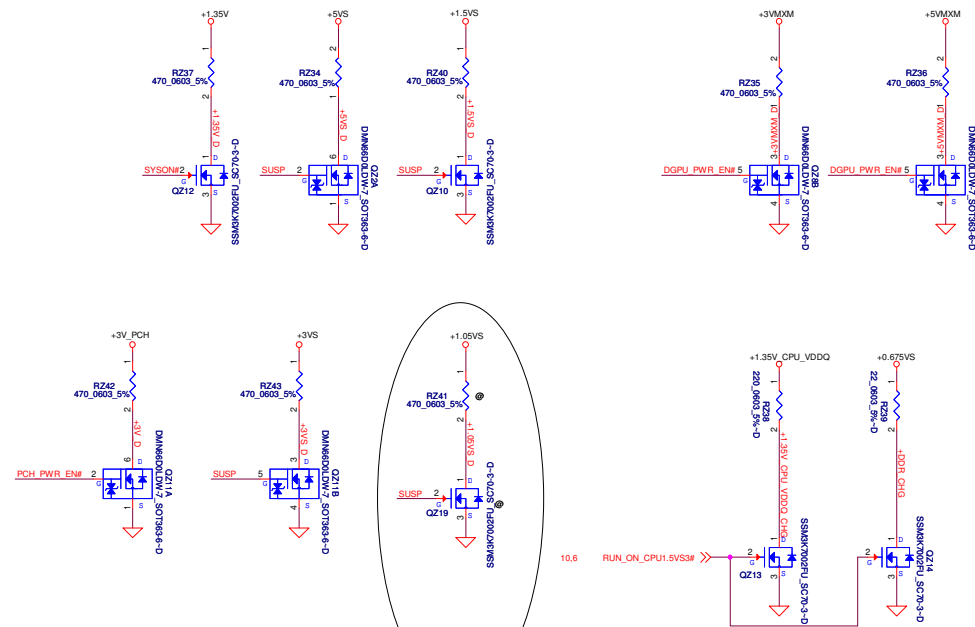


# Fiducial Mark

|   |            |                    |            |                                 |                |
|---|------------|--------------------|------------|---------------------------------|----------------|
| Security Classification   |            | Compal Secret Data |            | Title                           |                |
| Issued Date   | 2012/05/28 | Deciphered Date    | 2013/05/27 | KB & Power Button & IR          |                |
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|   |            |                    |            | Document Number                 | 0.1            |
|   |            |                    |            | LA-9332P                        |                |
|   |            |                    |            | Date: Friday, December 14, 2012 | Sheet 55 of 56 |

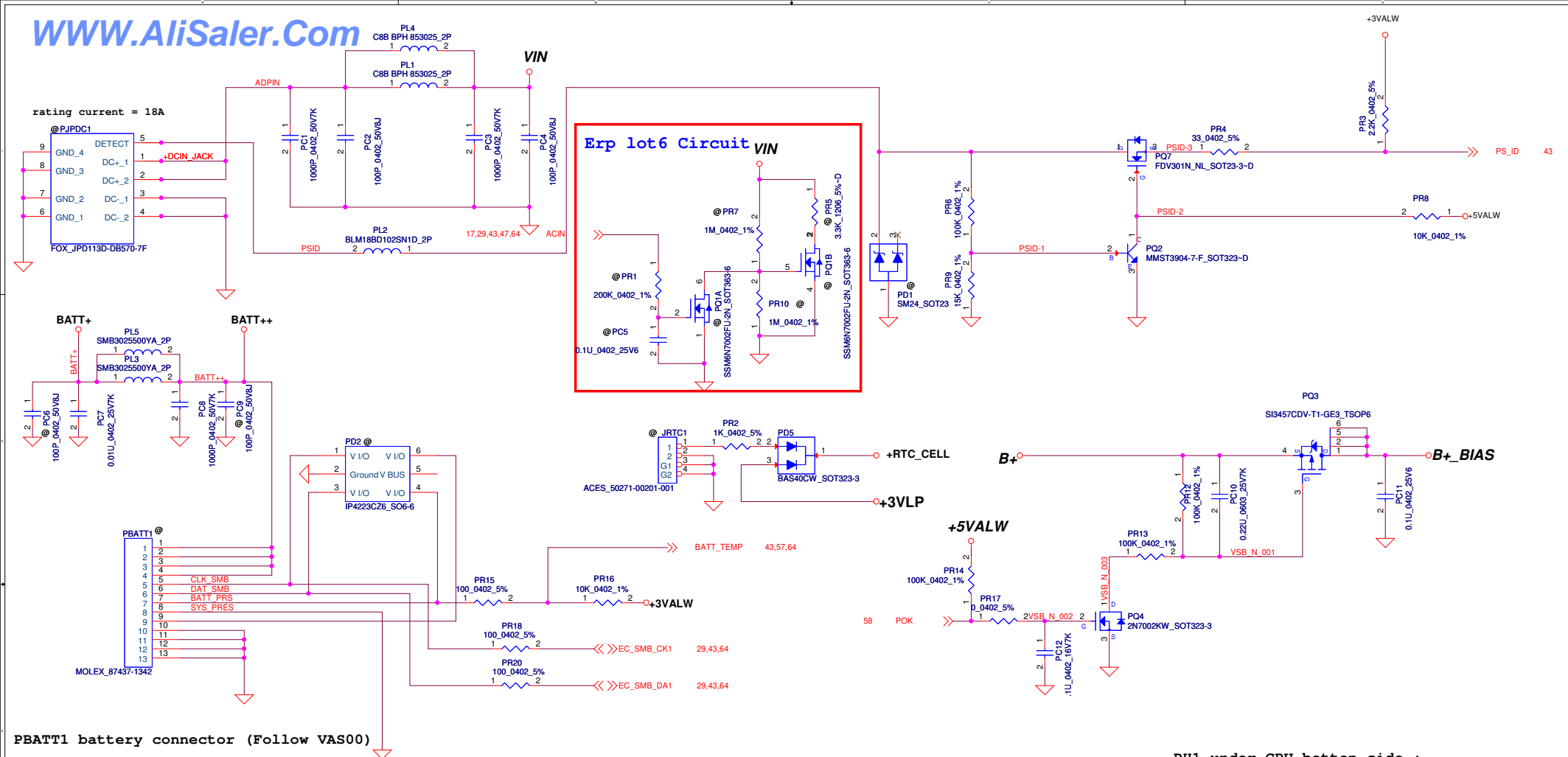


## Discharge Circuit



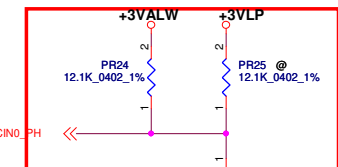
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| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc. |                           |                |
| Issued Date   | 2012/05/28         | Deciphered Date | 2013/05/27 | Title                    | DC/DC Interface           |                |
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|   |                    |                 |            | LA-932P                  | 0.1                       |                |
|   |                    |                 |            | Date:                    | Friday, December 14, 2012 | Sheet 56 of 56 |

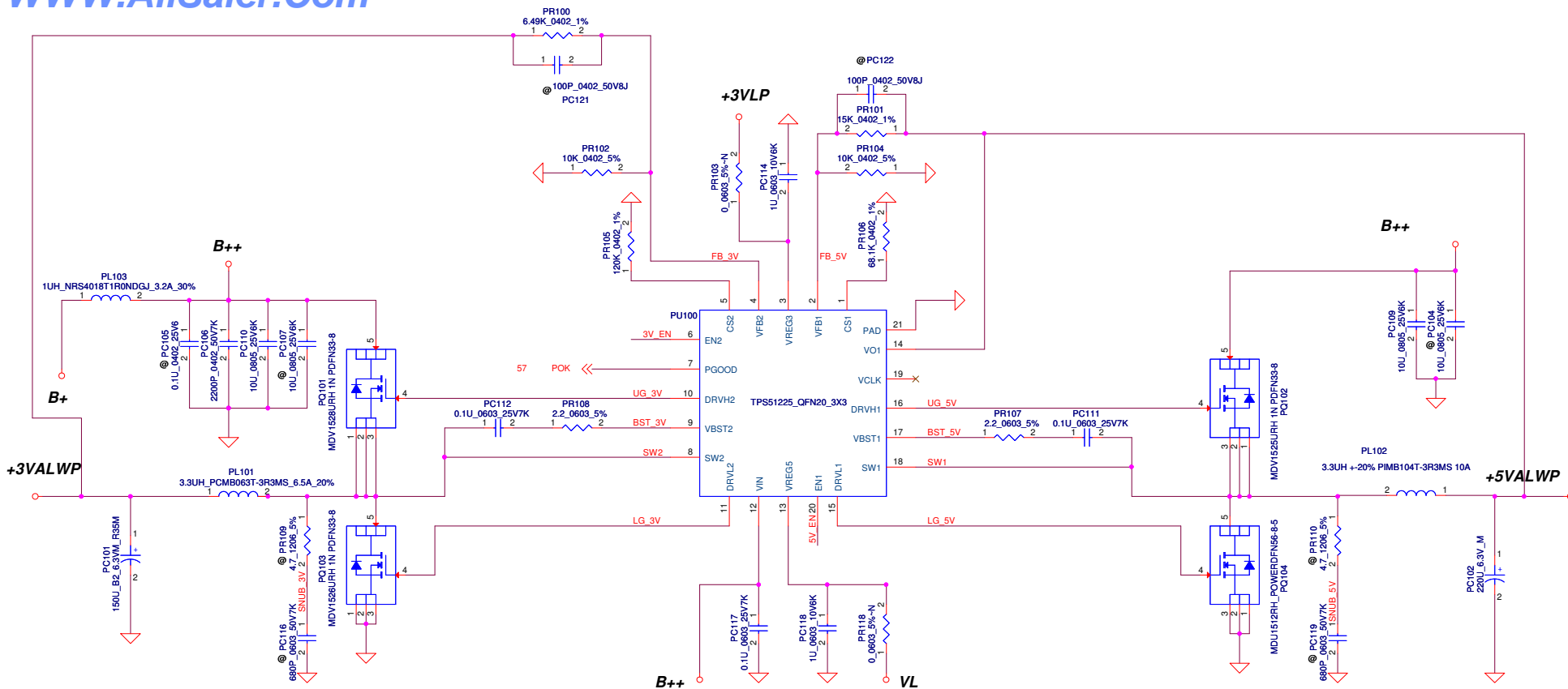




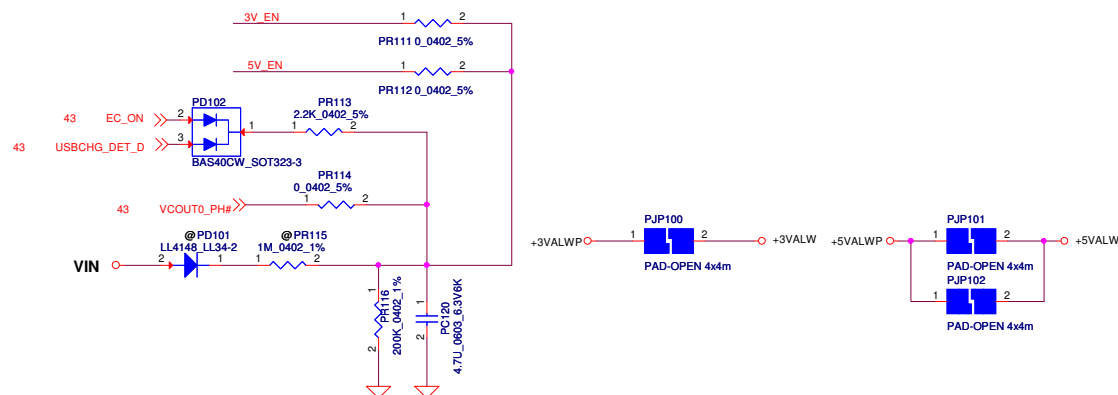
PH1 under CPU bottom side :  
CPU thermal protection at 93 +/- 3 degree C

| Adapter | ADP_SEL |
|---------|---------|
| 240W    | LOW     |
| 330W    | HIGH    |



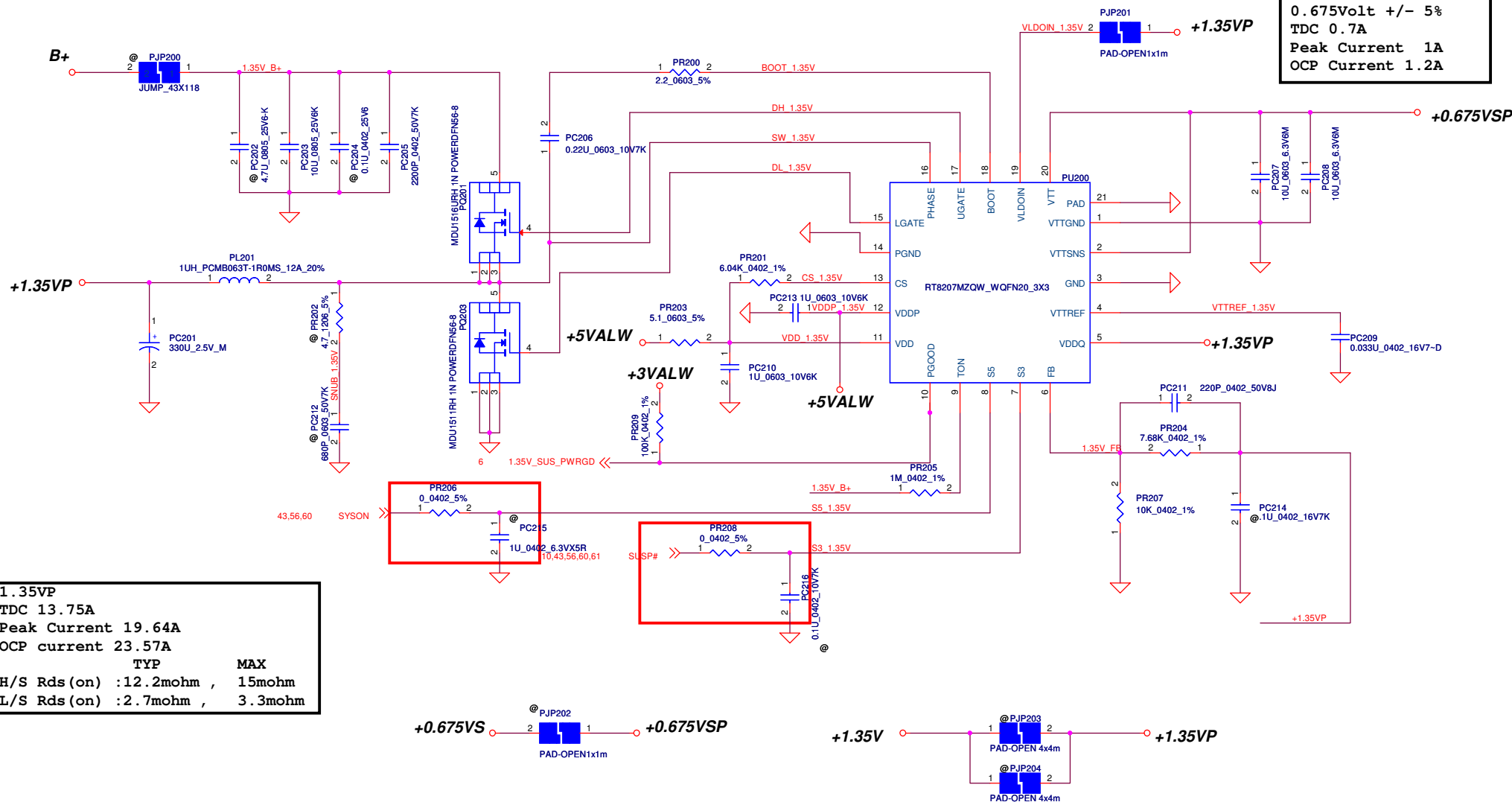


**3VALWP**  
TDC 6.08A  
Peak Current 8.11A  
OCP current 9.73A  
TYP MAX  
H/S Rds (on) 11.2mohm , 14mohm  
L/S Rds (on) 3.7mohm , 5mohm

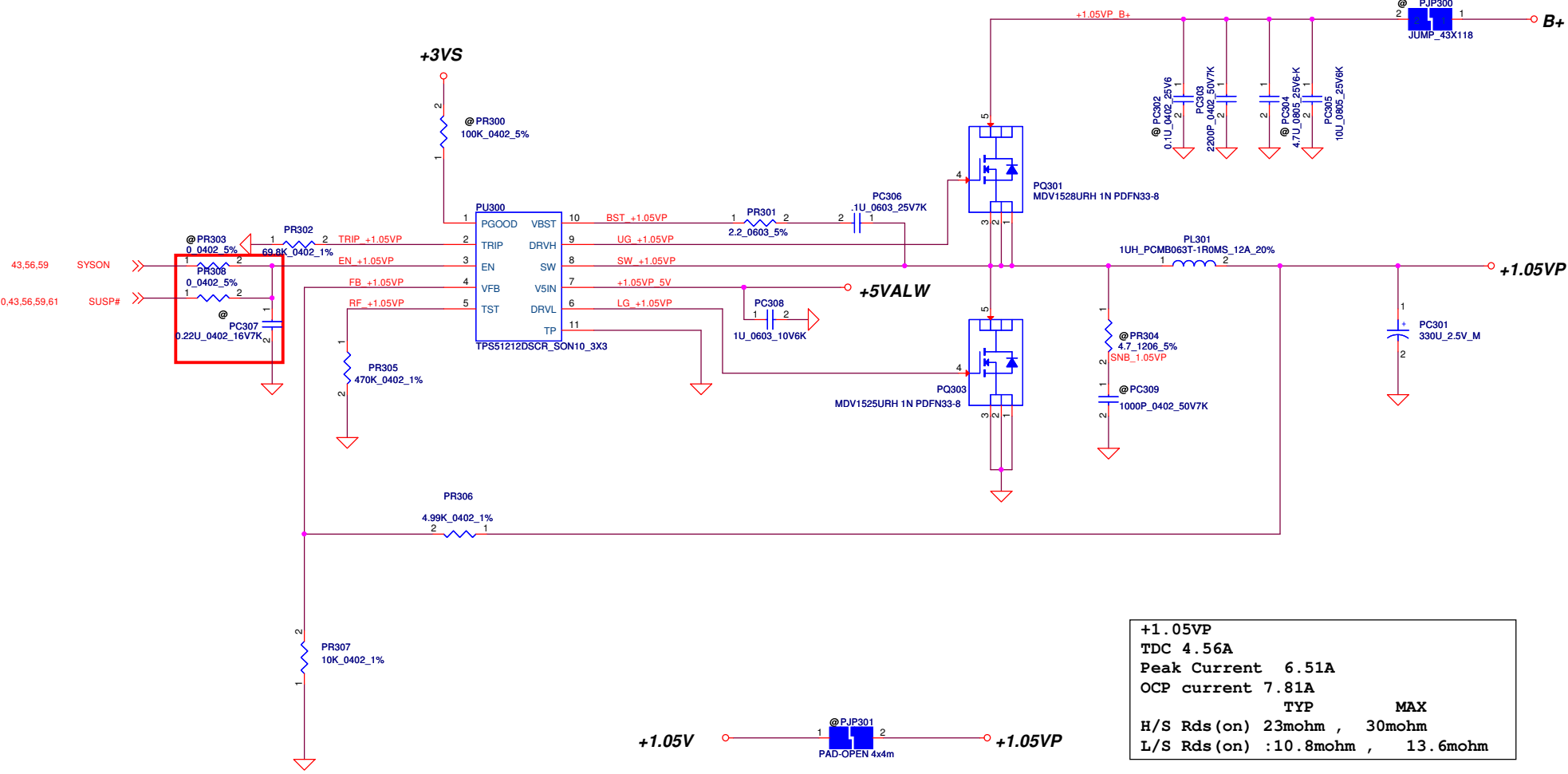


**5VALWP**  
TDC 11A  
Peak Current 16A  
OCP current 20A  
TYP MAX  
H/S Rds (on) 11.2mohm , 14mohm  
L/S Rds (on) 3.7mohm , 5mohm

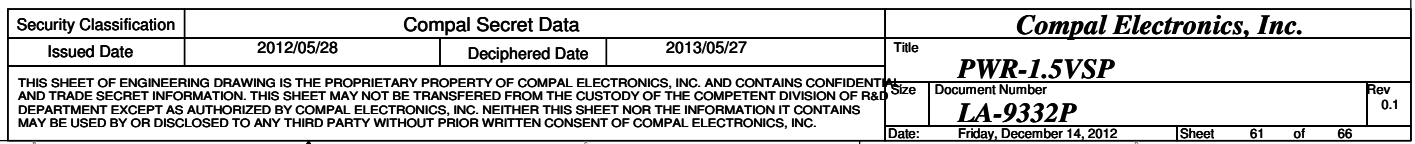
| Security Classification  | Compal Secret Data |                 | Title      |                 |
|--|--------------------|-----------------|------------|-----------------|
| Issued Date  | 2012/05/28         | Deciphered Date | 2013/05/27 | Document Number |
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| PWR-3VALWP/SVALWP  |                    |                 |            | LA-9332P        |
| Date: Friday, December 14, 2012  |                    |                 |            | Sheet 58 of 66  |

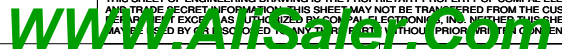


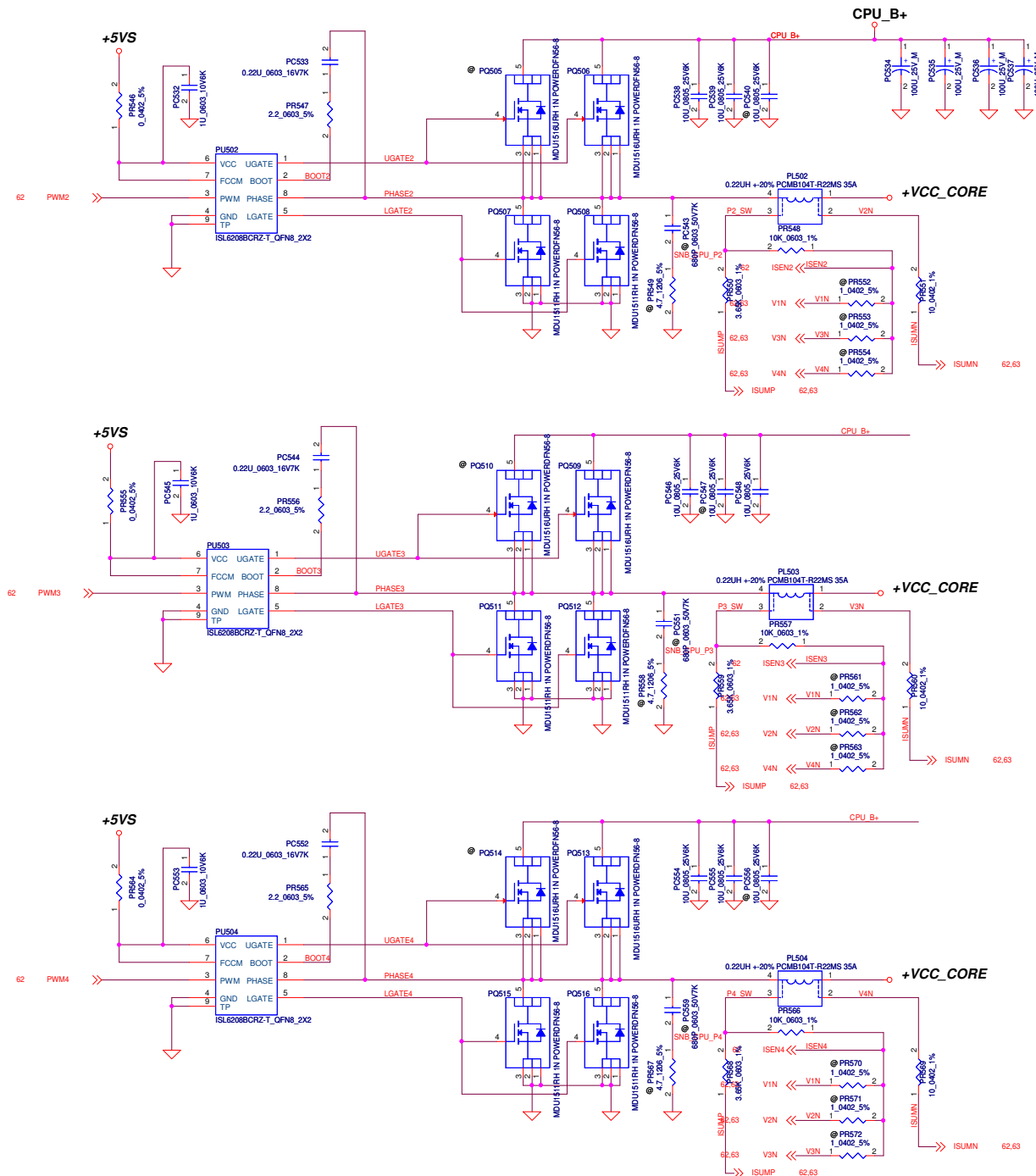
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| Security Classification  |                           | Compal Secret Data |            | Compal Electronics, Inc. |    |
| Issued Date  | 2012/05/28                | Deciphered Date    | 2013/05/27 | Title                    |    |
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| Size   | Document Number           | Rev                |            | LA-9332P                 |    |
| Date   | Friday, December 14, 2012 | Sheet              | 59         | of                       | 66 |



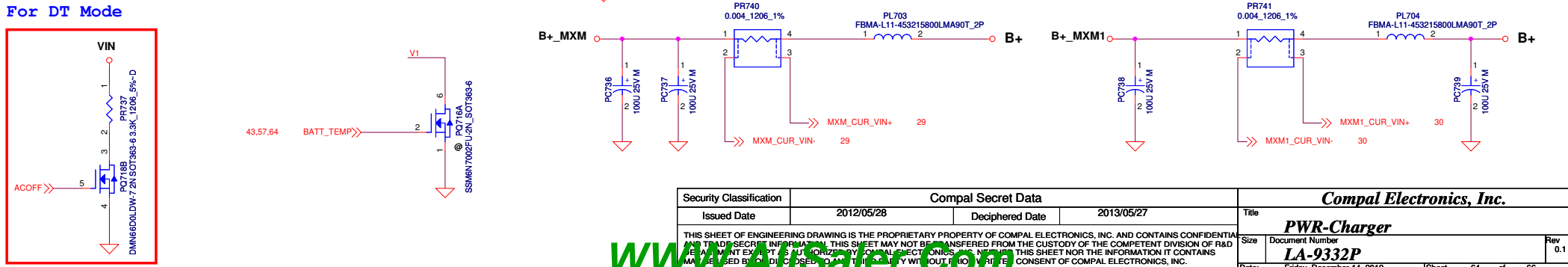
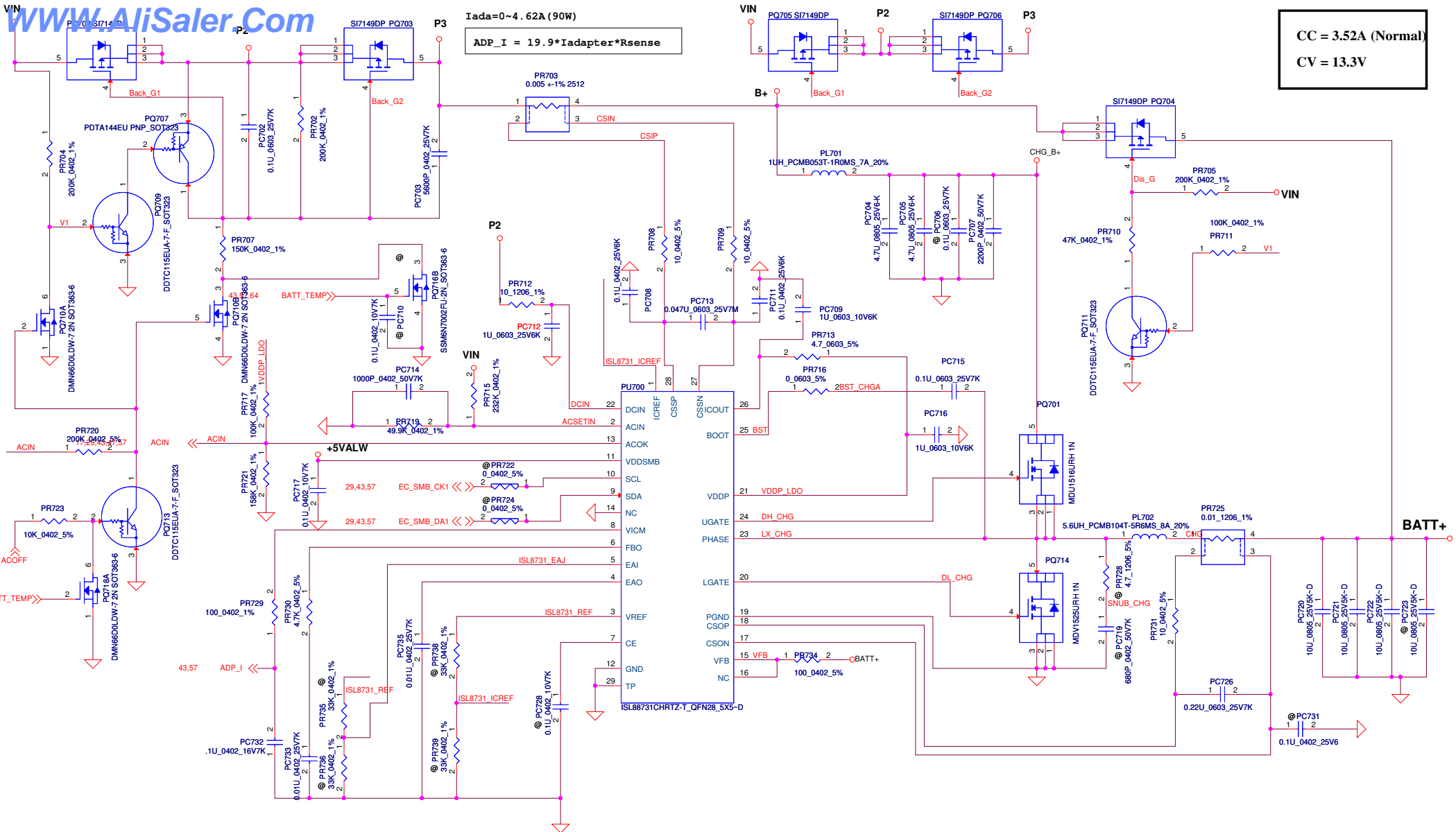
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| Security Classification  |            | Compal Secret Data |            | Compal Electronics, Inc. |                           |
| Issued Date  | 2012/05/28 | Deciphered Date    | 2013/05/27 | Title                    | PWR+1.05VP                |
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|  |            |                    |            | Date                     | Friday, December 14, 2012 |
|  |            |                    |            | Sheet                    | 60 of 66                  |
|  |            |                    |            | Rev                      | 0.1                       |





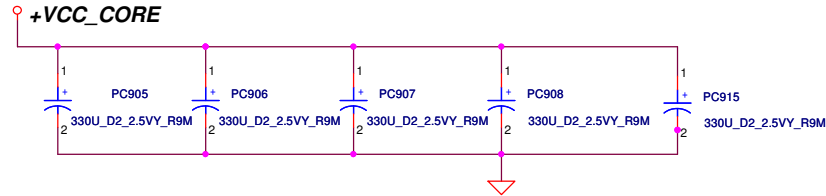
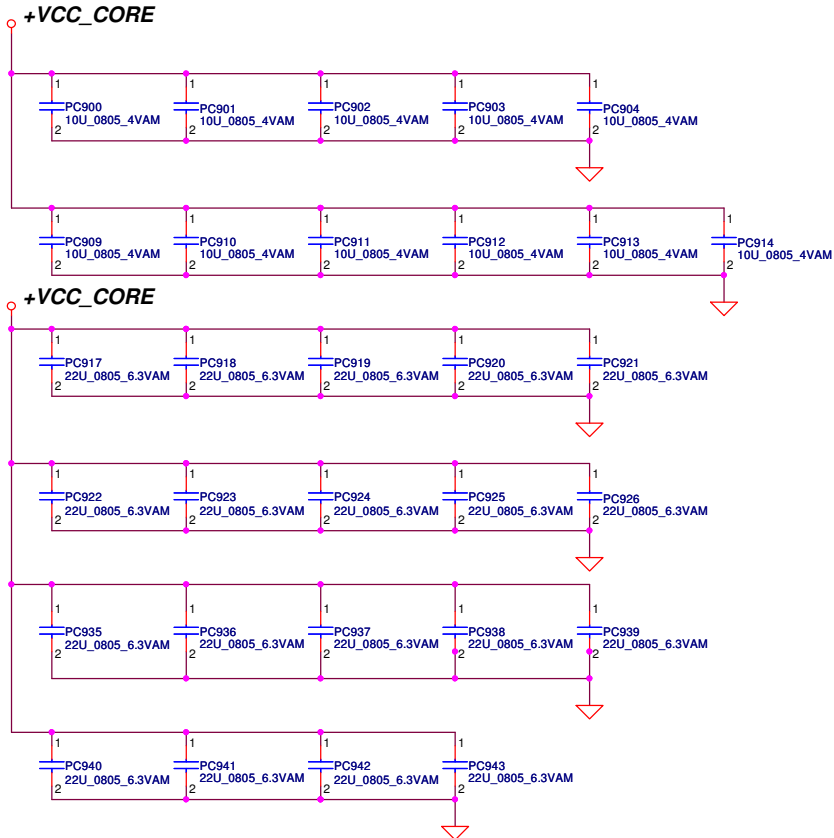


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|--|--------------------|-----------------|------------|--------------------------|---------------------------|
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|  |                    |                 |            |                          | Document Number           |
|  |                    |                 |            |                          | LA-9332P                  |
|  |                    |                 |            |                          | Rev                       |
|  |                    |                 |            |                          | 0.1                       |
|  |                    |                 |            |                          | Date                      |
|  |                    |                 |            |                          | Friday, December 14, 2012 |
|  |                    |                 |            |                          | Sheet                     |
|  |                    |                 |            |                          | 63 of 66                  |



|  |                 |                    |            |                          |                           |
|--|-----------------|--------------------|------------|--------------------------|---------------------------|
| Security Classification  |                 | Compal Secret Data |            | Compal Electronics, Inc. |                           |
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| Size   | Document Number | Rev                | 0.1        | Date                     | Friday, December 14, 2012 |
| LA-9332P   | Sheet           | 64                 | of         | 66                       |                           |






|  |                           |                    |            |                          |          |
|--|---------------------------|--------------------|------------|--------------------------|----------|
| Security Classification  |                           | Compal Secret Data |            | Compal Electronics, Inc. |          |
| Issued Date  | 2012/05/28                | Deciphered Date    | 2013/05/27 | Title                    |          |
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| Size   | Document Number           |                    |            | Rev                      |          |
|  | LA-9332P                  |                    |            | 0.1                      |          |
| Date:  | Friday, December 14, 2012 |                    |            | Sheet                    | 65 of 66 |

| Item | Reason for change  | Rev. | PG# | Modify List   | Date      | Phase |
|------|--|------|-----|---|-----------|-------|
| 1    | Adjust 1.5V output volatge                                   |      | P61 | change PR402 to 30.1K_0402_1%<br>PR405 to 20K_0402_1%                             | 2012.7.30 | SSI   |
| 2    | Adjust 3.3V OCP seeting                                      |      | P58 | change PR105 to 120K_0402_1%.   | 2012.7.30 | SSI   |
| 3    | Adjust 3V/5V always OTP seeting                              |      | P58 | modify PD100 to PR114 0_0402_1%.  | 2012.7.30 | SSI   |
| 4    | Adjust Vcore OTP seeting                                     |      | P62 | PR531 connect to +5VS   | 2012.7.30 | SSI   |
| 5    | Add PD3 PD4 for EMD requirement                              |      | P57 | add PD3 PD4 to PESD24VS2UT_SOT23-3  | 2012.8.16 | SSI   |
| 6    | hiccup mode issue is not happen so we haven't need solution. |      | P57 | remove Erp lot6 Circuit   | 2012.8.16 | SSI   |
| 7    | change diode for EMI requirement                             |      | P57 | use PD2 (6 PIN) to combine combine PD3(2PIN) PD4(2PIN ).                          | 2012.8.31 | SSI   |
| 8    | adjust the component for the 88731 schematic                 |      | P64 | change PR722 and PR724 to short footprint<br>remove PR701 PR706 PC701 PC734 PR732 | 2012.9.10 | SSI   |
| 9    | adjust RTC circuit for safety concern                        |      | P57 | add PR2 1K_0402_5%  | 2012.9.10 | SSI   |
| 10   | change ACIN bead for current limit rating                    |      | P57 | change PL1 PL4 to C8B BPH 853025_2P   | 2012.9.10 | SSI   |
| 11   | add PR116 for 3v 5v_EN delay time solution                   |      | P58 | add PR116 402K_0402_1%  | 2012.9.18 | SSI   |
| 12   | change output choke to improve efficiency                    |      | P59 | change PL201 to 1UH_PCMC063T-1R0MN  | 2012.9.18 | SSI   |
| 13   | change PR500 value to meet INTEL SPEC.                       |      | P62 | change PR500 to 130_0402_1%-D   | 2012.10.4 | SSI   |
|      |  |      | P67 |   |           |       |
| 14   |  |      |     |   |           |       |
| 15   |  |      |     |   |           |       |
| 16   |  |      |     |   |           |       |
| 17   |  |      |     |   |           |       |

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